

Clock Generator 0.001MHz to 3.25GHz-IN 3250MHz-OUT 64-Pin WQFN EP T/R



Images are for reference only

Manufacturer: [Texas Instruments, Inc](#)

Package/Case: QFN64

Product Type: Clock & Timer ICs

RoHS: RoHS Compliant/Lead free 

Lifecycle: Active

[Inquiry](#)

General Description

The LMK04832 is an ultra-high performance clock conditioner with JEDEC JESD204B support and is also pin compatible with the LMK0482x family of devices.

The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high performance outputs for traditional clocking systems.

The LMK04832 can be configured for operation in dual PLL, single PLL, or clock distribution modes with or without SYSREF generation or reclocking. PLL2 may operate with either internal or external VCO.

The high performance combined with features like the ability to trade off between power and performance, dual VCOs, dynamic digital delay, and holdover make the LMK04832 ideal for providing flexible high performance clocking trees.

Key Features

Maximum Clock Output Frequency: 3255 MHz

Multi-Mode: DualPLL, Single PLL, and Clock Distribution

Ultra-Low Noise, at 2500MHz:

54 fs RMS Jitter (12 kHz to 20 MHz)

64 fs RMS Jitter (100 Hz to 20 MHz)

-157.6 dBc/Hz Noise Floor

Ultra-Low Noise, at 3200 MHz:

61fs RMS Jitter (12 kHz to 20 MHz)

67 fs RMS Jitter (100 Hz to 100MHz)

-156.5 dBc/Hz Noise Floor

PLL2

PLL FOM of -230 dBc/Hz

PLL 1/f of -128dBc/Hz

Phase Detector Rate up to 320 MHz

Two Integrated VCOs: 2440 to 2580 MHz and 2945 to 3255 MHz

Up to 14 Differential Device Clocks

CML, LVPECL, LCPECL, HSDS, LVDS, and 2xLVCMOS Programmable Outputs

Up to 1 Buffered VCXO/XO Output

LVPECL, LVDS, 2xLVCMOS Programmable

1-1023 CLKout Divider

1-8191 SYSREF Divider

25-ps Step Analog Delay for SYSREF Clocks

Digital Delay and Dynamic Digital Delay for Device Clock and SYSREF

Holdover Mode With PLL1

0-Delay with PLL1 or PLL2

Supports 105°C PCB Temperature (Measured at Thermal Pad)

All trademarks are the property of their respective owners.

Recommended For You

LMK00334RTVR

Texas Instruments, Inc

WQFN32

LMC555CM

Texas Instruments, Inc

SOP8

LM555CM

Texas Instruments, Inc

SOP8

LMC555CMX/NOPB

Texas Instruments, Inc
SOP8

LM555CN

Texas Instruments, Inc
DIP8

LM555J/883

Texas Instruments, Inc
CDIP8

LMC555CMMX

Texas Instruments, Inc
MSOP8

LM555CN/NOPB

Texas Instruments, Inc
DIP8

LMC555CMMX/NOPB

Texas Instruments, Inc
VSSOP8

LMK00101SQE/NOPB

Texas Instruments, Inc
WQFN32

LM555H/883

Texas Instruments, Inc
CAN

LMK1C1102DQFR

Texas Instruments, Inc
WSO8-8

LMC555CN

Texas Instruments, Inc
DIP

LMC555IMX/NOPB

Texas Instruments, Inc
SOP8

LMC555CTP

Texas Instruments, Inc
DSBGA