PTN36502/PTN36502A

Type-C USB 3.1 Gen 1 and DisplayPort v1.2 combo redriver

Rev. 3 — 28 September 2018 Product data sheet

1 General description

PTN36502/PTN36502A is a Type-C USB 3.1 Gen 1/ DP1.2 combo redriver that is optimized for USB 3.1 Gen 1 and DisplayPort applications on either the Downstream Facing Port (DFP) or Upstream Facing Port (UFP) by following the four high-speed differential data flows to extend the signal reach.

PTN36502/PTN36502A addresses high-speed signal quality enhancement requirements for implementation of a USB Type-C interface in a platform that supports the VESA DisplayPort Alt Mode Standard v1.0a, includes a DisplayPort Branch or Sink function.

PTN36502/PTN36502A has three ternary (3-level) configuration pins (SCL/C1, SDA/C2 and EN), and depending on the state of EN pin during Power-On Reset (POR), the device gets into GPIO mode or I^2C mode. When EN is driven LOW during POR, PTN36502/PTN36502A operates under GPIO mode, and these three ternary pins are used to configure DFP/UFP configuration followed by mode setting (USB 3.1 Gen 1 and DisplayPort TX and RX function selection), as well as selecting receive equalization, transmit de-emphasis and output swing level. To support applications that require greater level of configurability, PTN36502/PTN36502A can operate in I^2C mode when EN pin is left open (OPEN/NC) during POR.

For DisplayPort (DP) operation, PTN36502/PTN36502A has a built-in internal crossbar function that can swap AUXP and AUXN signals for supporting plug orientation. PTN36502/PTN36502A monitors the AUX transactions and adjusts the DisplayPort transmitter's output swing and emphasis setting during DP Link training accordingly.

PTN36502/PTN36502A has built-in advanced power management capability that enables significant power saving under USB 3.1 Gen 1 Low power modes (U2/U3). It can detect LFPS signaling and link electrical conditions and can dynamically activate/deactivate internal circuitry and logic. The device performs these actions without host software intervention and conserves power. The host processor keeps PTN36502/PTN36502A in deep power saving or USB operation mode until DP Alt mode is entered.

PTN36502/PTN36502A is powered from a 1.8 V supply and it is available in an extremely thin HX2QFN24 package with 2.4 mm x 3.2 mm x 0.35 mm and 0.4 mm pitch.

2 Features and benefits

- Flexible Type-C USB/DP combo redriver supports four signaling combinations specified in USB Type-C and VESA DisplayPort Alt Mode Standards through either I^2C slave interface or ternary GPIO pins
  - Mode 1: One USB 3.1 Gen 1 port only
  - Mode 2: One USB 3.1 Gen 1 port + 2 lane DP + AUX channel
  - Mode 3: 4 lane DP + AUX channel
- Supports USB 3.1 Gen 1 data rate of 5 Gbps, and DisplayPort data rates at 1.62 Gbps, 2.7 Gbps and 5.4 Gbps (HBR2), AUX at 1 Mbps
- Compliant to SuperSpeed USB 3.1 Gen 1 standard
- Compliant to DisplayPort v1.2 standard for DFP applications
- Compliant to VESA DisplayPort Alt mode on USB Type-C standard
- Implements USB Type-C Safe state conditions on all connector facing pins
- Configurable via ternary GPIO or I^2C interface (operating up to 1 MHz)
- PTN36502 7-bit I^2C address = 001 1010
- PTN36502A 7-bit I^2C address = 001 0010
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- RX equalizers on all inputs to compensate for high speed signal attenuation in PCB and cable channels
- Active TX De-emphasis and Output swing on all outputs to assure high frequency boost
- Automatic Receiver Termination Detection in USB 3.1 Gen 1 mode
- Supports auto power saving modes during USB 3.1 Gen 1 operation
- DP AUX sideband crossbar switch for Type-C plug orientation
- DP AUX monitoring during DP link training to control DP TX output driver adjustment
- Flow-through pinout to ease PCB layout and minimize crosstalk effects
  - Low crosstalk: DDNEXT < -45 dB at 2.7 GHz
- Low active current consumption
  - USB 3.1 Gen 1 only (Mode 1) active power: 115 mA (typ) for VOS = 1Vpp and DE=-3.5 dB
  - 2-lane DP HBR2 level 0 (Mode 3): 75 mA (Level 0 : 400 mV with no Pre-emphasis)
  - 1-lane DP HBR2 level 0 (Mode 3): 38 mA (Level 0 : 400 mV with no Pre-emphasis)
  - 4-lane DP only HBR2 level 0 (Mode 3): 150 mA
- Power-saving states:
  - USB 3.1 Gen 1 mode (mode 1):
    - 1.16 mA (typ) when in USB 3.1 Gen 1 U2/U3 states
    - 0.77 mA (typ) when no connection detected (USB Rx detection enabled) (when a USB Type-C to USB Type-A adapter is connected to a USB Type-C port, but no USB Type-A device is attached to the adapter)
  - DP sleep D3 mode (Mode 2/3): 0.5 mA (typ)
  - 3 µA (typ) when in deep power-saving state
- Excellent Differential and Common return loss performance
- Hot Plug capable
- Single Power Supply 1.8 V
- Extremely thin HX2QFN24 package
  - 2.4 mm x 3.2 mm x 0.35 mm with 0.4 mm pitch

- ESD HBM 8 kV CDM 1 kV on high speed pins and HBM 4 kV CDM 500 V on control pins
- Supports IEC61000-4-5 8/20 µs ±16 V Surge test performance with external 4.7 Ω series resistors on the DRX1P/N, DRX2P/N and DAUXP/N pins
- Operating temperature range -40 to +85 ℃

3 Applications

- For USB Type-C Host/Source application
  - Smartphones and Tablets
  - Notebooks, AIO and Desktop Computers
  - Hub or Dock Devices
- For USB Type-C Device/Sink application
  - Docking Stations
  - Display units

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PTN36502HQ[1]	502	HX2QFN24	plastic, thermal enhanced super thin quad flat package; no leads; 24 terminals; 0.4 mm pitch, 2.4 mm x 3.2 mm x 0.35 mm body	SOT1903-1
PTN36502AHQ[2]	52A	HX2QFN24	plastic, thermal enhanced super thin quad flat package; no leads; 24 terminals; 0.4 mm pitch, 2.4 mm x 3.2 mm x 0.35 mm body	SOT1903-1

[1] PTN36502 7-bit I^2C address = 001 1010
[2] PTN36502A 7-bit I^2C address = 001 0010

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN36502HQ[1]	PTN36502HQX	HX2QFN24	REEL 7" Q1/T1 *STANDARD MARK SMD	3000	T_{amb} = -40 °C to 85 °C
PTN36502AHQ[2]	PTN36502AHQX	HX2QFN24	REEL 7" Q1/T1 *STANDARD MARK SMD	3000	T_{amb} = -40 °C to 85 °C

[1] PTN36502 7-bit I^2C address = 001 1010
[2] PTN36502A 7-bit I^2C address = 001 0010

5 Functional diagram

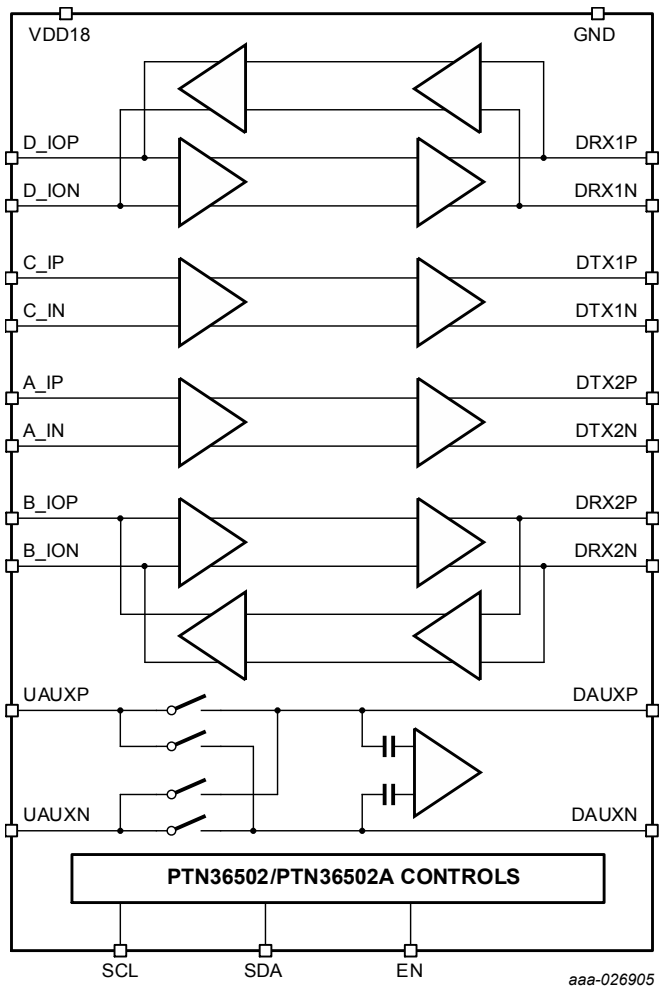


Figure 1. Functional diagram

6 Pinning information

6.1 Pinning

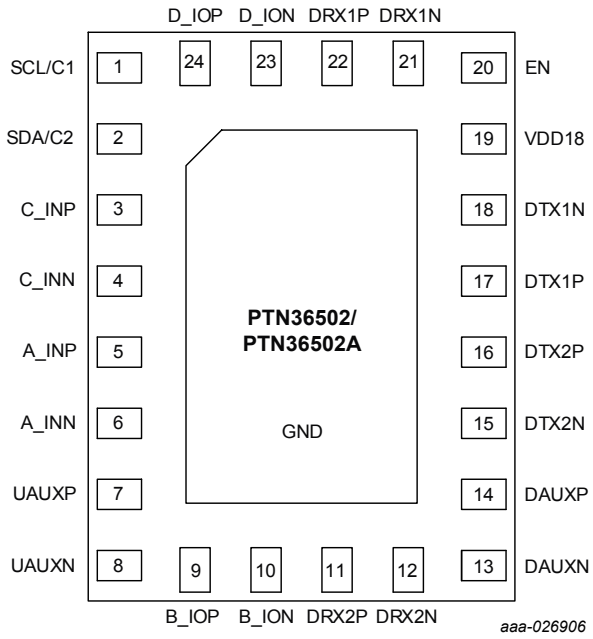


Figure 2. PTN36502/PTN36502A pinning (transparent top view)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
1	SCL/C1	Ternary open drain input/ output	When PTN36502/PTN36502A is operating in I^2C mode, this pin is slave I^2C clock pin, and external pull-up resistor to 1.8 V or 3.3 V is required. When PTN36502/PTN36502A is operating in GPIO mode, this pin has multiple functions depending on EN pin state, and is 1.8 V tolerant. Refer to Section 7.6 for more details.
2	SDA/C2	Ternary open drain input/ output	When PTN36502/PTN36502A is operating in I^2C mode, this pin is slave I^2C data pin, and external pull-up resistor to 1.8 V or 3.3 V is required. When PTN36502/PTN36502A is operating in GPIO mode, this pin has multiple functions depending on EN pin state, and is 1.8 V tolerant. Refer to Section 7.6 for more details.
3	C_INP	Self-biasing differential input	Differential signal from high speed RX path. C_IP makes a differential pair with C_IN. The associated TX output pair is DTX1P and DTX1N
4	C_INN		
5	A_INP	Self-biasing differential input	Differential signal from high speed RX path. A_IP makes a differential pair with A_IN. The associated TX output pair is DTX2P and DTX2N
6	A_INN		
7	UAUXP	I/O	Upstream AUX Channel I/O. When PTN36502/PTN36502A is placed in DFP application, these signals should be AC coupled as per DP spec
8	UAUXN		

Symbol	Pin	Type	Description
9	B_IOP	Self-biasing differential input/output	Differential signal high speed input/output. B_IOP makes a differential pair with B_ION. The associated output/input pair is DRX2P and DRX2N. The I/O configuration is controlled by mode setting
10	B_ION		
11	DRX2P	Self-biasing differential input/output	Differential signal high speed input/output. DRX2P makes a differential pair with DRX2N. The associated output/input pair is B_IOP and B_ION. The I/O configuration is controlled by mode setting
12	DRX2N		
13	DAUXN	I/O	Downstream AUX Channel I/O. When PTN36502/PTN36502A is placed in UFP application, these signals should be AC coupled as per DP spec
14	DAUXP		
15	DTX2N	Self-biasing differential output	Differential signal of high speed TX path. DTX2P makes a differential pair with DTX2N. The associated RX input pair is A_IP and A_IN
16	DTX2P		
17	DTX1P	Self-biasing differential output	Differential signal of high speed TX path. DTX1P makes a differential pair with DTX1N. The associated RX input pair is C_IP and C_IN
18	DTX1N		
19	VDD18		1.8 V Supply
20	EN	Ternary input	3 level mode configuration pin. When power is applied on VDD18 pin • If EN = 0, PTN36502/PTN36502A is operating in GPIO mode • If EN = OPEN, PTN36502/PTN36502A is operating in I^2C mode
21	DRX1N	Self-biasing differential input/output	Differential signal high speed input/output. DRX1P makes a differential pair with DRX1N. The associated output/input pair is D_IOP and D_ION. The I/O configuration is controlled by mode setting
22	DRX1P		
23	D_ION	Self-biasing differential input/output	Differential signal high speed input/output. D_IOP makes a differential pair with D_ION. The associated output/input pair is DRX1P and DRX1N. The I/O configuration is controlled by mode setting
24	D_IOP		
Center pad	GND		The center pad must be connected to GND plane for both electrical grounding and thermal relief

7 Functional description

7.1 USB 3.1 Gen 1 operation

PTN36502/PTN36502A supports USB redriver operation at 5 Gbps. The receive equalization, transmit output swing and de-emphasis settings are configured via GPIO or I^2C register settings.

PTN36502/PTN36502A has implemented an advanced power management scheme that operates in tune with USB 3.1 Gen 1 Bus electrical condition. Though the device does not decode USB power management commands (related to USB 3.1 Gen 1 U1/ U2/U3 transitions) exchanged between USB Host and Peripheral/Device, it relies on bus electrical conditions and control pins/register settings to decide to be in one of the following states:

- Active state wherein device is fully operational. In this state, USB connection exists and the Receive Termination remains active.
- Power-saving state wherein some portions of the TX and RX channels are kept enabled. In this state, squelching, LFPS detection and/or Receive termination detection circuitry are active. Based on USB connection, there are two possibilities:
  - No USB connection (also called Rx-detect state)
    - Receive Termination detection circuitry keeps polling periodically
    - RX and TX signal paths (including squelch detector) are not enabled
    - Receive Termination is not active
    - DC Common mode voltage level is not maintained
  - When USB connection exists and when the link is in USB U2/U3 mode,
    - Receive Termination detection circuitry keeps polling periodically
    - RX and TX signal paths are not enabled; squelch detector is enabled
    - Receive Termination is active
    - DC Common mode voltage level is maintained

7.2 DisplayPort v1.2 operation

PTN36502/PTN36502A supports DisplayPort redriver operation at 1.62 Gbps, 2.7 Gbps and 5.4 Gbps, with 2-tap pre-emphasis, pre-emphasis levels 0 to 3 and output swing levels 0 to 3.

The DisplayPort mode is selected only when DP Alternate mode has been entered by the host controller. Until then, PTN36502/PTN36502A stays in deep power saving or USB 3.1 Gen 1 only mode. The DisplayPort source can activate power down via AUX command.

The DisplayPort link rate, lane count, transmit output swing and pre-emphasis settings are configured autonomously during DisplayPort link training phase based on AUX communication exchanges between Source and Sink. In addition, the host can configure these settings via I^2C interface.

Table 4 illustrates the various combinations allowed and supported in DisplayPort modes. The host AP shall configure the settings only based on valid combinations listed in this table. Note PTN36502/PTN36502A does not check if combination is valid while being configured.

Table 4. Allowed output swing and pre-emphasis combinations in DisplayPort mode

Output swing level	Pre-emphasis level			
	0 (0 dB)	1 (3.5 dB)	2 (6 dB)	3 (8.8 dB)
0 (400 mV)	Supported	Supported	Supported	Supported
1 (600 mV)	Supported	Supported	Supported	Not allowed
2 (800 mV)	Supported	Supported	Not allowed	Not allowed
3 (1100 mV)	Supported	Not allowed	Not allowed	Not allowed

It is possible that only a subset of lanes gets selected during DP Link training and remaining lanes are not active. Depending on the number of lanes selected, PTN36502/PTN36502A is configured to operate with the selected lane count thereby saving power consumption on unused lanes.

7.2.1 AUX crossbar switch

PTN36502/PTN36502A implements AUX crossbar switch with low insertion loss and R_{ON}. All AUX traffic is passively passed through from one side to another. The switch can be configured for 'pass through' mode or 'pass through with cross' mode. The host processor can configure the switch via GPIO or I^2C-bus interface. By default, the switch is in Hi-Z state at power-on reset.

7.2.2 AUX monitoring and configuration

PTN36502/PTN36502A monitors DP AUX communication exchanges that occur between DP source and DP sink and passes the AUX data in either direction (Source to sink and Sink to source). In particular, it detects for AUX communication involving DPCD register controls – Lane count, Link rate, Transmit output swing, Transmit pre-emphasis level, Sleep, Wake, etc. and configures its operation suitably. It also performs inversion as required for plug orientation in DFP configurations. At DP AUX PHY level, the required local biasing and AC coupling capacitance are implemented.

When PTN36502/PTN36502A is placed in DFP mode, the polarity of internal AUX monitoring signal follows the orientation of the cable connector plugged in. For example, if the orientation is reversed on the Type-C connector, signals presented on DAUXP and DAUXN pins will be interpreted as AUXN and AUXP signals internally.

When PTN36502/PTN36502A is placed in UFP mode, the polarity of internal AUX monitoring signal is fixed regardless of orientation of cable connector plugged in. Signals presented on DAUXP and DAUXN pins are interpreted as AUXP and AUXN signals internally.

The list of DPCD registers (with only the relevant bit fields) supported are as follows:

- LINK_BW_SET
- LANE_COUNT_SET
- TRAINING_LANEx_SET (x=0-3) (the DP source issues this command after sending the specific training pattern and so, the redriver must target very small delay)
- SET POWER
- Other DPCD registers and I^2C over AUX transactions are not decoded

The applied values are expected to be within the capabilities of PTN36502/PTN36502A.

In case GPU sends out LANE_COUNT_SET =0 during AUX training, it is necessary to program I^2C register 0x06 to value of 0x06 after entering DP modes (either mode 2 or 3).

This will ensure the PTN36502/PTN36502A DisplayPort starts up properly. Please follow PTN36502/PTN36502A programming guide.

7.3 USB Type-C DFP receptacle application

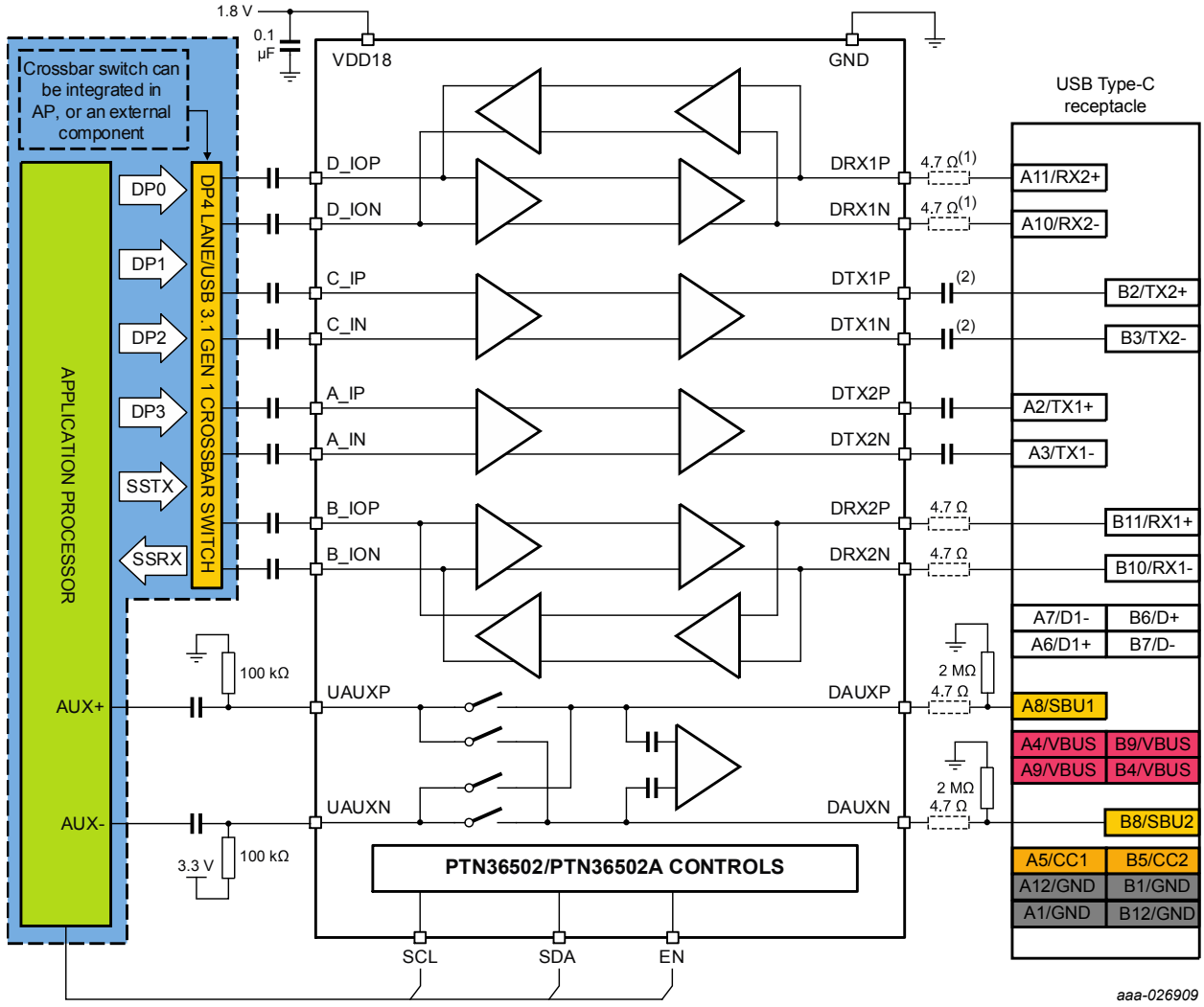


Figure 3. Connection illustration when PTN36502/PTN36502A in DFP receptacle application

(1): 0.33µF capacitors are recommended on Type-C's receiver pins based on latest USB specification.
(2): 0.22µF capacitors are recommended on Type-C's transmitter pins based on latest USB specification.

Refer to Figure 3 for using PTN36502/PTN36502A in USB Type-C DFP receptacle application. In this configuration, upstream (left) side of PTN36502/PTN36502A is connected to application processor with integrated or on-board crossbar switch function, and downstream (right) side is connected to Type-C receptacle.

Each pin on the downstream side of PTN36502/PTN36502A connecting to the Type-C connector has specific input/output configuration, and must match the signal assignments on the upstream side accordingly. Table 5 shows the downstream pin connection to Type-C receptacle.

Table 5. Downstream pin connection to Type-C receptacle in DFP application

PTN36502/PTN36502A pins		USB Type-C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
22	DRX1P	A11	RX2+
21	DRX1N	A10	RX2-
18	DTX1N	B3	TX2-
17	DTX1P	B2	TX2+
16	DTX2P	A2	TX1+
15	DTX2N	A3	TX1-
12	DRX2N	B10	RX1-
11	DRX2P	B11	RX1+
14	DAUXP	A8	SBU1
13	DAUXN	B8	SBU2

The upstream pins of PTN36502/PTN36502A are connected to the application processor, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN36502/PTN36502A controls which transmitters or receivers to turn on or turn off, and operating in USB 3.1 Gen 1 mode, or DisplayPort mode according to the mode setting.

Table 6. Upstream pin connection to application processor in DFP receptacle application

PTN36502/ PTN36502A pins	Application processor signal names						
Symbol	**Pin name**	**USB 3.1 Gen 1**		**USB 3.1 Gen 1 and DP2Lane**		**DP4Lane**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
23	D_ION		SSRX-	ML0-	SSRX-	ML0-	ML3-
24	D_IOP		SSRX+	ML0+	SSRX+	ML0+	ML3+
3	C_INP		SSTX+	ML1+	SSTX+	ML1+	ML2+
4	C_INN		SSTX-	ML1-	SSTX-	ML1-	ML2-
5	A_INP	SSTX+		SSTX+	ML1+	ML2+	ML1+
6	A_INN	SSTX-		SSTX-	ML1-	ML2-	ML1-
9	B_IOP	SSRX+		SSRX+	ML0+	ML3+	ML0+
10	B_ION	SSRX-		SSRX-	ML0-	ML3-	ML0-
7	UAUXP			AUX+	AUX+	AUX+	AUX+
8	UAUXN			AUX-	AUX-	AUX-	AUX-

7.4 USB Type-C UFP receptacle application

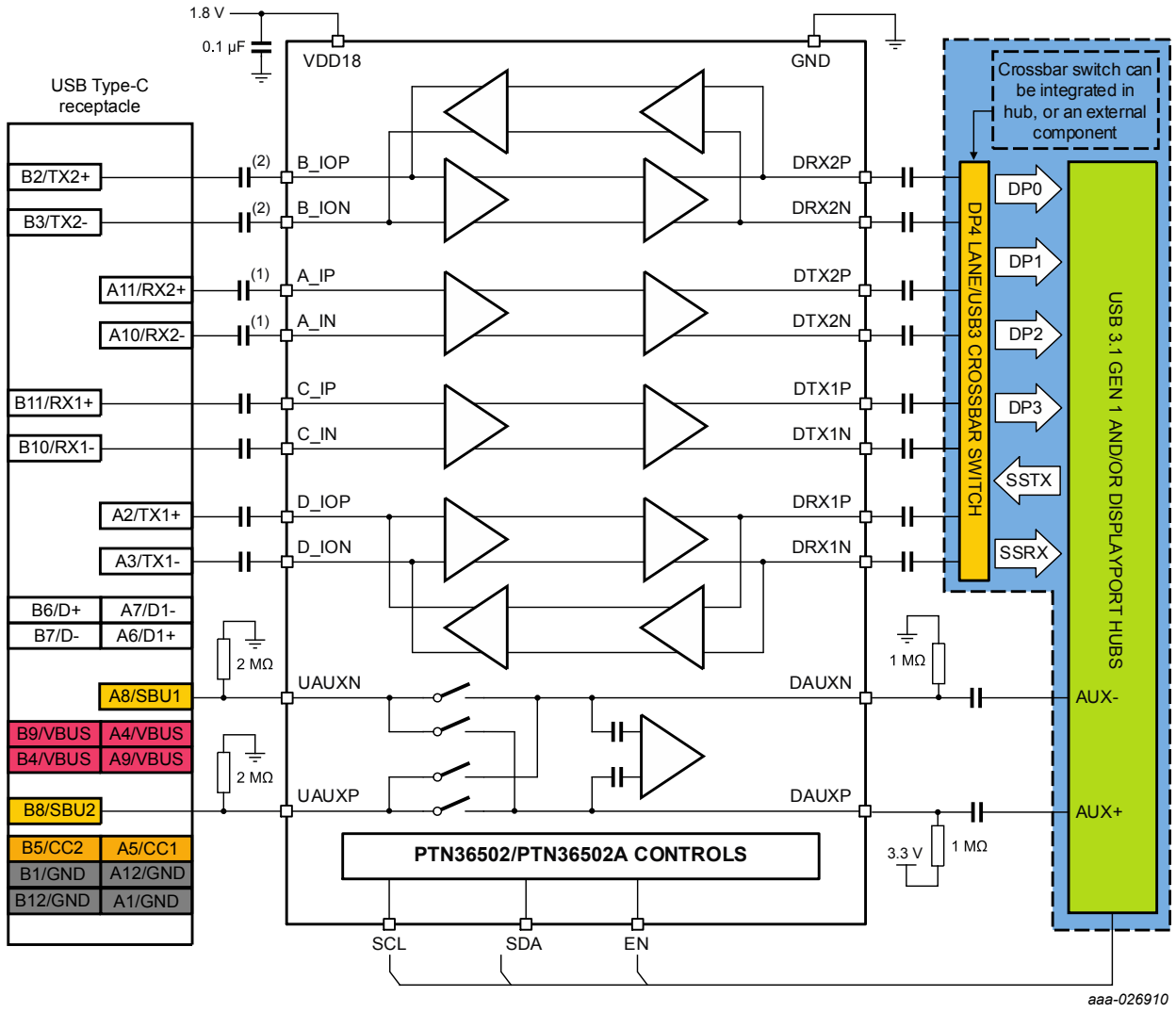


Figure 4. Connection illustration when PTN36502/PTN36502A in UFP receptacle application

(1): 0.33µF capacitors are recommended on Type-C's receiver pins based on latest USB specification.

(2): 0.22µF capacitors are recommended on Type-C's transmitter pins based on latest USB specification.

Refer to Figure 4 for using PTN36502/PTN36502A in USB Type-C UFP receptacle application. In this configuration, downstream (right) side of PTN36502/PTN36502A is connected to USB 3.1 Gen 1 and/or DisplayPort hubs with integrated or on-board crossbar switch function, and upstream (left) side is connected to Type-C receptacle.

Each pin on the upstream side of PTN36502/PTN36502A connecting to the Type-C connector has specific input/output configuration, and must match the signal assignments on the downstream side accordingly. Table 7 shows the upstream pin connection to Type-C receptacle.

Table 7. Upstream pin connection to Type-C receptacle in UFP application

PTN36502/PTN36502A pins		USB Type-C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
23	D_ION	A3	TX1-
24	D_IOP	A2	TX1+
3	C_INP	B11	RX1+
4	C_INN	B10	RX1-
5	A_INP	A11	RX2+
6	A_INN	A10	RX2-
9	B_IOP	B2	TX2+
10	B_ION	B3	TX2-
7	UAUXP	B8	SBU2
8	UAUXN	A8	SBU1

The downstream pins of PTN36502/PTN36502A are connected to the USB 3.1 Gen 1 and/or DisplayPort hubs, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN36502/PTN36502A controls which transmitters or receivers to turn on or turn off, and operating in USB 3.1 Gen 1 mode, or DisplayPort mode according to the mode setting.

Table 8. Downstream pin connection to USB 3.1 Gen 1/DisplayPort hubs in UFP receptacle application

PTN36502/PTN36502A pins	Hub signal names						
Symbol	**Pin name**	**USB 3.1 Gen 1**		**USB 3.1 Gen 1 and DP2Lane**		**DP4Lane**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
22	DRX1P	SSTX+		SSTX+	ML0+	ML3+	ML0+
21	DRX1N	SSTX-		SSTX-	ML0-	ML3-	ML0-
18	DTX1N	SSRX-		SSRX-	ML1-	ML2-	ML1-
17	DTX1P	SSRX+		SSRX+	ML1+	ML2+	ML1+
16	DTX2P		SSRX+	ML1+	SSRX+	ML1+	ML2+
15	DTX2N		SSRX-	ML1-	SSRX-	ML1-	ML2-
12	DRX2N		SSTX-	ML0-	SSTX-	ML0-	ML3-
11	DRX2P		SSTX+	ML0+	SSTX+	ML0+	ML3+
14	DAUXP			AUX+	AUX+	AUX+	AUX+
13	DAUXN			AUX-	AUX-	AUX-	AUX-

7.5 USB Type-C UFP_Dongle application

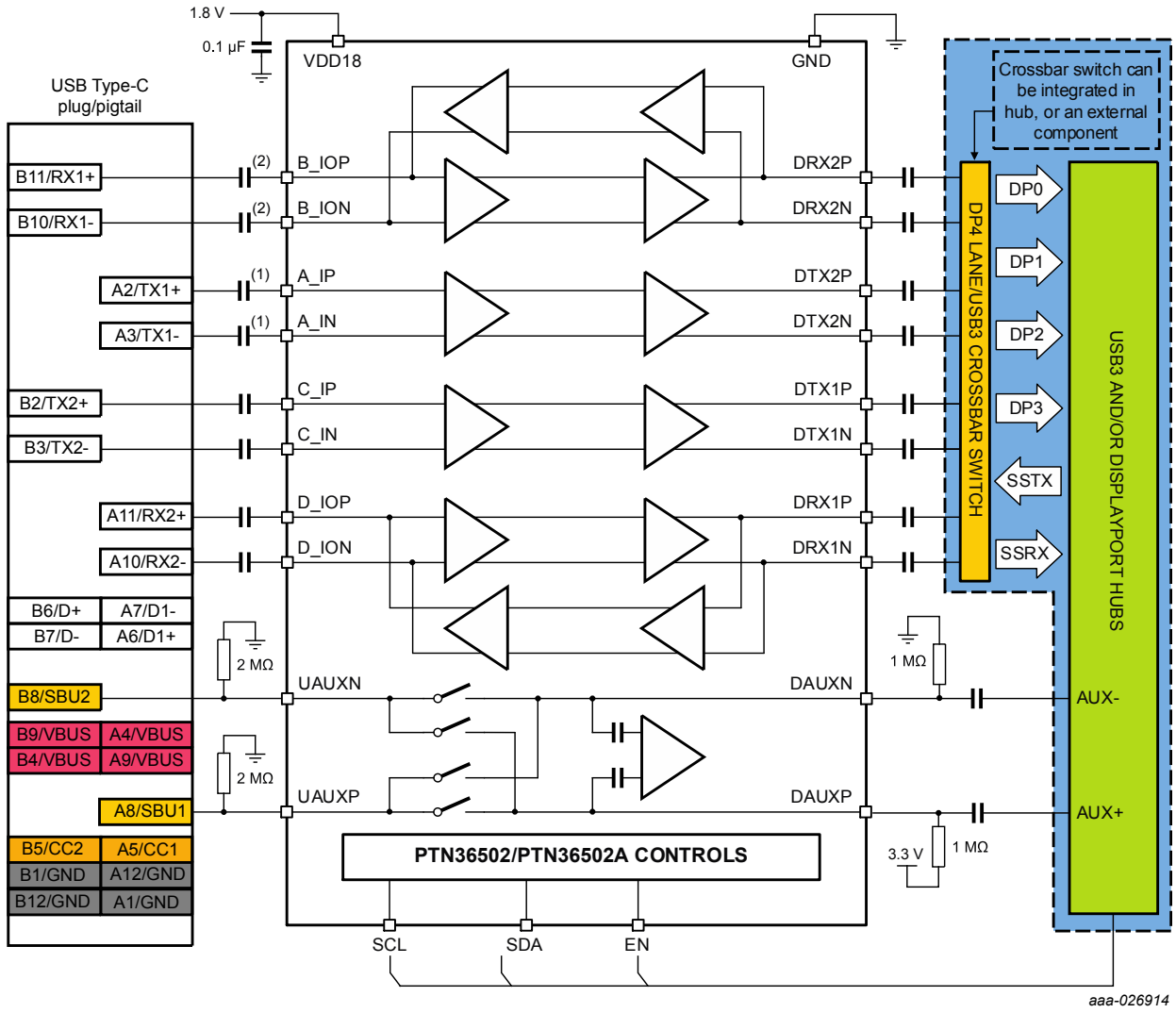


Figure 5. Connection illustration when PTN36502/PTN36502A in UFP_Dongle application

(1): 0.33µF capacitors are recommended on Type-C's receiver pins based on latest USB specification.
(2): 0.22µF capacitors are recommended on Type-C's transmitter pins based on latest USB specification.

Refer to Figure 5 for using PTN36502/PTN36502A in USB Type-C UFP_Dongle application. In this configuration, downstream (right) side of PTN36502/PTN36502A is connected to USB 3.1 Gen 1 and/or DisplayPort hubs with integrated or on-board crossbar switch function, and upstream (left) side is connected to Type-C plug.

Each pin on the upstream side of PTN36502/PTN36502A connecting to the Type-C connector has specific input/output configuration, and must match the signal assignments on the downstream side accordingly. Table 9 shows the upstream pin connection to Type-C plug.

Table 9. Upstream pin connection to Type-C plug UFP_Dongle application

PTN36502/PTN36502A pins		USB Type-C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
23	D_ION	A10	RX2-
24	D_IOP	A11	RX2+
3	C_INP	B2	TX2+
4	C_INN	B3	TX2-
5	A_INP	A2	TX1+
6	A_INN	A3	TX1-
9	B_IOP	B11	RX1+
10	B_ION	B10	RX1-
7	UAUXP	A8	SBU1
8	UAUXN	B8	SBU2

The downstream pins of PTN36502/PTN36502A are connected to the USB 3.1 Gen 1 and/or DisplayPort hubs, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN36502/PTN36502A controls which transmitters or receivers to turn on or turn off, and operating in USB 3.1 Gen 1 mode, or DisplayPort mode according to the mode setting.

A typical dongle has a fixed orientation design, usually the normal orientation. Therefore, only one CC line is connected on the USB Type-C plug, and the other CC line is being used for VCONN purpose. PTN36502/PTN36502A offers both normal and reversed orientation pin outs, and can be adapted to different layout requirements. However, in a typical dongle use case, only one orientation is necessary.

Table 10. Downstream pin connection to USB 3.1 Gen 1/DisplayPort hubs in UFP_Dongle application

PTN36502/ PTN36502A pins	Hub signal names						
Symbol	**Pin name**	**USB 3.1 Gen 1**		**USB 3.1 Gen 1 and DP2Lane**		**DP4Lane**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
22	DRX1P		SSTX+	ML0+	SSTX+	ML0+	ML3+
21	DRX1N		SSTX-	ML0-	SSTX-	ML0-	ML3-
18	DTX1N		SSRX-	ML1-	SSRX-	ML1-	ML2-
17	DTX1P		SSRX+	ML1+	SSRX+	ML1+	ML2+
16	DTX2P	SSRX+		SSRX+	ML1+	ML2+	ML1+
15	DTX2N	SSRX-		SSRX-	ML1-	ML2-	ML1-
12	DRX2N	SSTX-		SSTX-	ML0-	ML3-	ML0-
11	DRX2P	SSTX+		SSTX+	ML0+	ML3+	ML0+
14	DAUXP			AUX+	AUX+	AUX+	AUX+
13	DAUXN			AUX-	AUX-	AUX-	AUX-

7.6 Control and programmability

PTN36502/PTN36502A implements ternary control IO logic on EN, C1/SCL, C2/SDA control pins to detect HIGH (connected to VDD), LOW (connected to GND) or left unconnected condition (OPEN/NC). These pins are 3.3 V tolerant in I^2C mode, and 1.8 V tolerant in GPIO mode.

The following sections describe the individual block functions and capabilities of the device in more detail. In general, depending on the EN transition, there are specific functions for each transition state. Figure 6 and Figure 7 illustrate transitions described above. Hi-Z and OPEN/NC are used interchangeably in these figures.

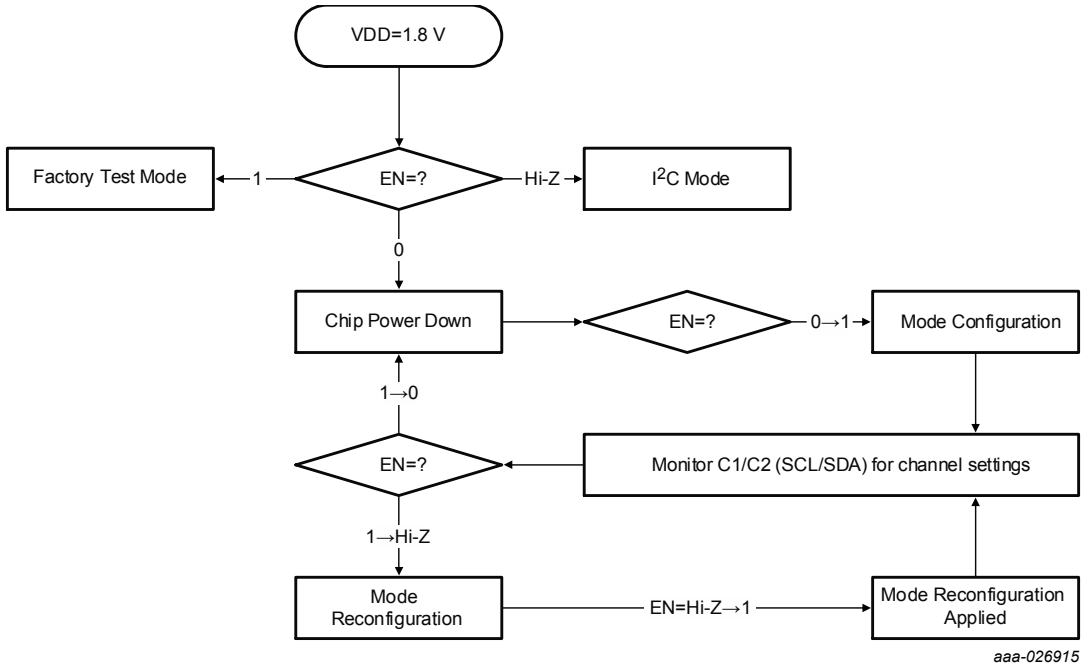


Figure 6. GPIO mode control flow chart

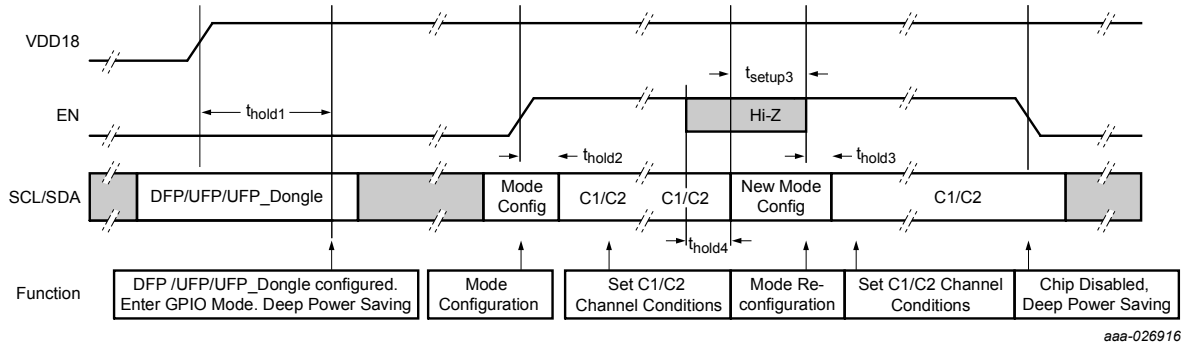


Figure 7. GPIO mode control sequence diagram illustration

7.6.1 Operating mode selection (I^2C mode or GPIO mode)

Upon POR, PTN36502/PTN36502A starts to detect the state of EN pin. If EN is not driven (or left OPEN) during POR, PTN36502/PTN36502A defaults to operate in I^2C mode, and EN pin has no function after entering I^2C mode. In I^2C mode, PTN36502/PTN36502A is highly programmable. For more information, please reference Section 7.6.6 for I^2C register details.

If EN is driven LOW during POR (through a GPIO from host processor or external pull down resistor), the PTN36502/PTN36502A will be placed in GPIO mode. At the same time, PTN36502/PTN36502A is configured in DFP, UFP, or UFP_Dongle modes depending on SCL/C1 and SDA/C2 pins' status (refer to Table 11 below). By default, the chip is disabled in deep power saving mode after DFP/UFP/UFP_Dongle configuration is detected. In the deep power saving mode, all PTN36502/PTN36502A line drivers and input receive paths are terminated to ground with hi-ohmic resistors and AUX switches are tri-stated, and mode configuration remains undetermined.

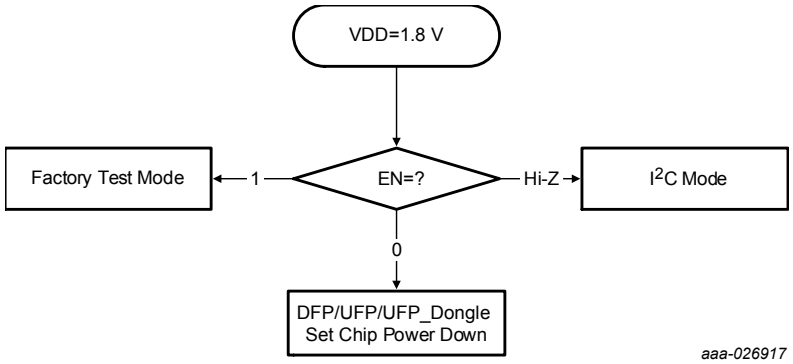


Figure 8. EN control flow diagram

Table 11. EN control for various mode setting during POR

EN	SCL/C1	SDA/C2	Mode
OPEN	X	X	I^2C Mode
0	0	0	GPIO Mode – DFP Configuration, without external 4.7 Ω resistors on the DRXn pins.
	0	1	GPIO Mode – DFP Configuration, with external 4.7 Ω resistors added on the DRXn pins for higher level surge protection.
	1	0	GPIO Mode – UFP Configuration.
	0	0	GPIO Mode – UFP_Dongle Configuration.
1	X	X	Reserved Operation Mode

7.6.2 Mode configuration through GPIO mode

Table 12, Table 13, and Table 14 show seven possible modes in which PTN36502/PTN36502A can be configured while operating in DFP, UFP, or UFP plug modes respectively. Note that mode configuration setting is latched when EN transition from 0 to 1. When the mode needs to be reconfigured (for example, change from USB 3.1 Gen 1+DP2Lane mode to DP4Lane mode) after EN is 1, a GPIO controller can toggle EN pin to Hi-Z first and back to high again with new mode presented on SCL/C1 and SDA/

C2 pins. New mode value is latched when EN transition from Hi-Z to 1, and may take up to 0.2 milliseconds to take effect. When EN is toggled back to 0, mode configuration is cleared, and the PTN36502/PTN36502A is placed in deep power saving mode.

- C1/SCL indicates the orientation, 0 = normal orientation, 1 = reversed orientation
- C2/SDA indicates different mode configurations
  - OPEN=USB 3.1 Gen 1 only, no AUX support
  - 0 = USB 3.1 Gen 1 + DP 2Lane + AUX
  - 1 = DP 4Lane + AUX

Definitions of different lane TX and RX paths in the tables are illustrated in Figure 9.

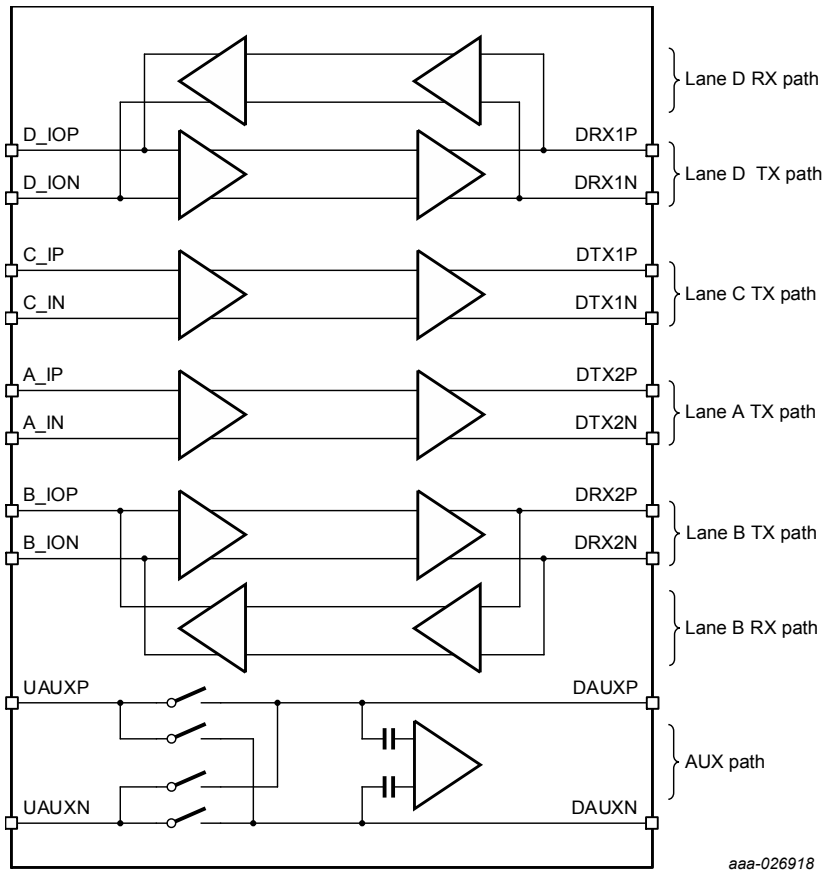


Figure 9. Different lane TX and RX paths definitions

Table 12. PTN36502/PTN36502A DFP mode configuration

EN	SCL/C1	SDA/ C2	Lane A TX	Lane B TX	Lane B RX	Lane C TX	Lane D TX	Lane D RX	AUX Path	Mode	Type-C orientation
Transition from 0 to 1	0	OPEN	SSTX		SSRX	[1]		[1]		USB 3.1 Gen 1 Only (M=1)	Normal (Or=0)
	1	OPEN	[1]		[1]	SSTX		SSRX			Reversed (Or=1)

EN	SCL/C1	SDA/ C2	Lane A TX	Lane B TX	Lane B RX	Lane C TX	Lane D TX	Lane D RX	AUX Path	Mode	Type-C orientation
	0	0	SSTX		SSRX	ML1	ML0		Thru	USB 3.1 Gen 1 & DP2 Lane (M=2)	Normal (Or=0)
	1	0	ML1	ML0		SSTX		SSRX	Cross		Reversed (Or=1)
	0	1	ML2	ML3		ML1	ML0		Thru	DP4 Lane (M=3)	Normal (Or=0)
	1	1	ML1	ML0		ML2	ML3		Cross		Reversed (Or=1)

[1] Unused TX and RX pins are terminated to ground with hi-ohmic resistors

Table 13. PTN36502/PTN36502A UFP mode configuration

EN	SCL/C1	SDA/ C2	Lane A TX	Lane B TX	Lane B RX	Lane C TX	Lane D TX	Lane D RX	AUX Path	Mode	Type-C orientation
Transition from 0 to 1	0	OPEN	[1]		[1]	SSRX		SSTX		USB 3.1 Gen 1 Only (M=1)	Normal (Or=0)
	1	OPEN	SSRX		SSTX	[1]		[1]			Reversed (Or=1)
	0	0	ML1	ML0		SSRX		SSTX	Thru	USB 3.1 Gen 1 & DP2 Lane (M=2)	Normal (Or=0)
	1	0	SSRX		SSTX	ML1	ML0		Cross		Reversed (Or=1)
	0	1	ML1	ML0		ML2	ML3		Thru	DP4Lane (M=3)	Normal (Or=0)
	1	1	ML2	ML3		ML1	ML0		Cross		Reversed (Or=1)

[1] Unused TX and RX pins are terminated to ground with hi-ohmic resistors

Table 14. PTN36502/PTN36502A UFP_Dongle mode configuration

EN	SCL/C1	SDA/ C2	Lane A TX	Lane B TX	Lane B RX	Lane C TX	Lane D TX	Lane D RX	AUX Path	Mode	Type-C orientation
Transition from 0 to 1	0	OPEN	SSRX		SSTX	[1]		[1]		USB 3.1 Gen 1 Only (M=1)	Normal (Or=0)
	1	OPEN	[1]		[1]	SSRX		SSTX			Reversed (Or=1)
	0	0	SSRX		SSTX	ML1	ML0		Thru	USB 3.1 Gen 1 & DP2 Lane (M=2)	Normal (Or=0)
	1	0	ML1	ML0		SSRX		SSTX	Cross		Reversed (Or=1)

EN	SCL/C1	SDA/ C2	Lane A TX	Lane B TX	Lane B RX	Lane C TX	Lane D TX	Lane D RX	AUX Path	Mode	Type-C orientation
	0	1	ML2	ML3		ML1	ML0		Thru	DP4 Lane (M=3)	Normal (Or=0)
	1	1	ML1	ML0		ML2	ML3		Cross		Reversed (Or=1)

[1] In USB 3.1 Gen 1 only mode, unused line drivers (TX) and input receivers (RX) are terminated to common mode (<2V) with hi-ohmic resistors

The AUX switch path remains enabled irrespective of DP lane sleep status as long as the mode is configured for DP support. The AUX switch path is disabled only during deep power saving state (when EN=0) or when mode is configured to USB 3.1 Gen 1 only mode (mode1).

7.6.3 Mode transitions

PTN36502/PTN36502A implements USB 3.1 Gen 1 (single port), and Combo (DP/USB) modes as per DP Alt mode specification. The mode transitions follow USB Safe state transition requirements of USB Type-C cable and Connection specification, USB Power Delivery and DisplayPort Alternate Mode specifications. Figure 10 illustrates the various functional modes and deep power saving state transitions.

By default/POR, PTN36502/PTN36502A enters deep power saving mode state. In deep power saving mode, all high-speed pins are put in safe state by pulling these pins to ground with internal hi-ohmic resistors. The AUX switch path is disabled and AUX/SBU pins can be put in safe state by pulling these to ground by means of hi-ohmic resistors in the application. When a valid Type-C cable is connected, the host PD controller can first place PTN36502/PTN36502A in USB 3.1 Gen 1 mode (mode 1). If DP Alt mode is negotiated, PTN36502/PTN36502A adheres to the USB safe state requirements before making the mode transition. Except for transitions from Mode 1 to Mode 2, all other transitions need to happen via deep power saving state in order to meet USB Safe state requirements.

When transitioning from Mode 1 to Mode 2, the USB 3.1 Gen 1 connectivity is left undisturbed and 2-lane DP + AUX functionality is included. It is advised not to transition from Mode 2 back to Mode 1 directly; internal power management scheme automatically places DisplayPort operation in low power state.

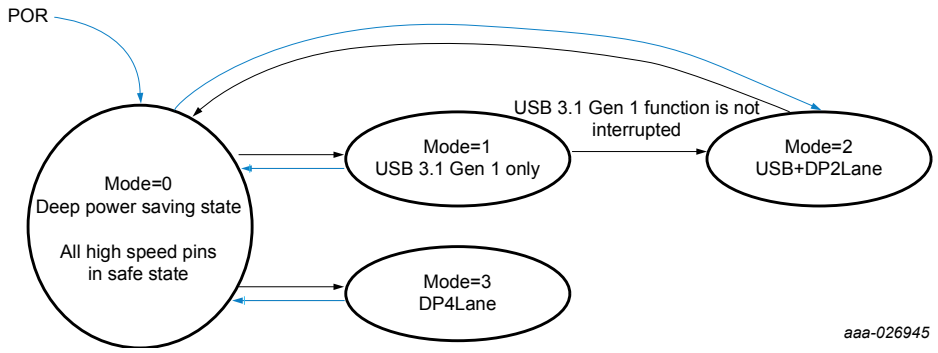


Figure 10. Mode transition state diagram

7.6.4 Channel settings for USB 3.1 Gen 1 mode

After EN pin is in steady state HIGH, C1/SCL and C2/SDA pins are used for upstream and downstream channel condition settings. PTN36502/PTN36502A samples these two pins every few milliseconds, and the configuration settings can be updated at any time, as long as EN is set to HIGH.

C1 controls signal traces on the upstream (left) side (as shown in Figure 3) of the redriver. It controls receive equalization, transmit de-emphasis and output swing interfacing pins with the host processor interface.

- When C1 = HIGH, the upstream (left) side of the redriver is optimized to drive long channel trace length
- When C1 = OPEN, the upstream (left) side of the redriver is optimized to drive medium channel trace length
- When C1 = LOW, the upstream (left) side of the redriver is optimized to drive short channel trace length

Table 15. Upstream channel configuration using C1 pin

C1 state	Channel type	Upstream RX	Upstream TX	
		EQ[1]	DE[2]	OS[3]
HIGH	Long	9 dB	-5.3 dB	1100 mV
OPEN	Medium	6 dB	-3.1 dB	1000 mV
LOW	Short	3 dB	0 dB	900 mV

[1] EQ is the input receiver equalization gain
[2] DE is the transmit output signal de-emphasis gain
[3] OS is the transmit output differential voltage

C2 controls signal traces on the downstream (right) side with functionality similar to C1 (as shown in Figure 3). These pins are the Type-C connector in a DFP system.

Table 16. Downstream channel configuration using C2 pin

C2 state	Channel type	Downstream RX	Downstream TX	
		EQ[1]	DE[2]	OS[3]
HIGH	Long	9 dB	-5.3 dB	1100 mV
OPEN	Medium	6 dB	-3.1 dB	1000 mV
LOW	Short	3 dB	0 dB	900 mV

[1] EQ is the input receiver equalization gain
[2] DE is the transmit output signal de-emphasis gain
[3] OS is the transmit output differential voltage

7.6.5 Channel settings for DisplayPort mode

In GPIO mode, lane count, link rate, transmit output and pre-emphasis settings are determined by AUX DPCD commands. Only the input receive equalization is determined by C1 value. C2 is not used.

Table 17. DisplayPort channel equalization settings

C1 state	Channel type	Upstream RX equalization		
		1.62 Gbps	2.7 Gbps	5.4 Gbps
HIGH	Long	4.5 dB	6 dB	9 dB
OPEN	Medium	1.5 dB	3 dB	6 dB
LOW	Short	0 dB	1.5 dB	3 dB

All lanes of DP redriver use the same setting in GPIO mode whereas they can be configured separately on a per lane basis. The transmit line driver output swing and pre-emphasis control settings are set based on AUX transactions during DP Link training and these can also be configured via I^2C-bus interface.

In I^2C mode, AUX monitor training can be disabled with full control of output swing, pre-emphasis and RX equalization through I^2C registers. If AUX monitor bit (in Register 0xoD) is enabled, the default value of output swing, pre-emphasis and RX equalization values will be based on the values in the I^2C registers. After AUX monitor training, output swing and pre-emphasis will be adjusted; the RX equalization value is not modified.

7.6.6 I^2C configurability

PTN36502/PTN36502A has an I^2C register interface that enables system integrator to program register settings suitable as per application needs. Table 18 describes possible settings for different functions of the device. Though the device can be pin configured through board-strapping or it also allows the system integrator to override those settings by programming the registers through I^2C.

After power-on, the device samples EN pin and if it is OPEN, the device defaults to operate in I^2C mode. The system integrator must program the registers of the device for proper operation. Further, it is expected that the system integrator performs I^2C configuration after power-on and before data transport is initiated over the link. If such an operation is attempted during normal operation, the device may not behave as specified.

Note that registers 0x06, 0x07, 0x08, 0x09 and 0x0A hold DP link settings can be modified by AUX monitor; therefore, these registers do not necessarily hold the latest settings that are applied to the DP channel training through AUX.

Table 18. I^2C registers and description

Register offset	Register name	Bits	POR default value	Description
0x00 Read Only	Chip ID	7:0	b'0000 0010	Chip ID Number
0x01 Read Only	Chip Revision	7:4	b`0001	Chip base layer version
		3:0	b`0010	Chip metal layer version
0x02-0x03	Reserved	7:0	Don't care	
0x04 Read/Write	USB_US_TX/RX_ Control	7:6	b`01	USB mode upstream (left) side link de-emphasis level • 0: de-emphasis = 0 dB • 1: de-emphasis = -3.1 dB • 2: de-emphasis = -5.3 dB • 3: Reserved

Register offset	Register name	Bits	POR default value	Description
		5:4	b`00	USB mode upstream (left) side link output signal swing • 0: output swing level = 900mVppd • 1: output swing level = 1000mVppd • 2: output swing level = 1100mVppd • 3: reserved
		3:0	b`0010	USB mode upstream (left) side link Rx Equalization gain • 0: 0 dB • 1: 3 dB • 2: 6 dB • 3: 9 dB • 4: 12 dB • 5-15: reserved
0x05 Read/Write	USB_DS_TX/RX_ Control	7:6	b`01	USB mode downstream (right) side link de-emphasis level • 0: de-emphasis = 0 dB • 1: de-emphasis = -3.1dB • 2: de-emphasis = -5.1 dB • 3: Reserved
		5:4	b`00	USB mode downstream (right) side link output signal swing • 0: output swing level = 900mVppd • 1: output swing level = 1000mVppd • 2: output swing level = 1100mVppd • 3: reserved
		3:0	b`0010	USB mode downstream (right) side link Rx Equalization gain • 0: 0 dB • 1: 3 dB • 2: 6 dB • 3: 9 dB • 4: 12 dB • 5-15: reserved
0x06 Read/Write	DP link control	7:5	b`000	Reserved
		4	b`0	DisplayPort Power saving mode selection on all DP lanes. • 0: Normal/Active mode • 1: D3 Power saving mode
		3:2	b`00	DisplayPort operating lane count. • 0: 0 DP Lane (i.e. USB 3.1 Gen 1 Only) • 1: 1 DP Lane • 2: 2 DP lanes • 3: 4 DP lanes

Register offset	Register name	Bits	POR default value	Description
		1:0	b`00	DP Link rate • 0: 1.62 Gbps (RBR) • 1: 2.7 Gbps (HBR) • 2: 5.4 Gbps (HBR2) • 3: Reserved.
0x07 Read/Write	DP Lane 0 TX/RX Control Register	7	b`0	Reserved
		6:4	b`000	DP Lane 0 Rx equalization gain control • 0: 0 dB • 1: 1.5 dB • 2: 3 dB • 3: 4.5 dB • 4: 6 dB • 5: 9 dB • 6: 12dB • 7: Reserved
		3:2	b`00	DP Lane 0 TX output swing control (When AUX monitor bit in 0x0D byte is disabled) • 0: 400 mVppd • 1: 600 mVppd • 2: 800 mVppd • 3: 1100mVppd
		1:0	b`00	DP Lane 0 pre-emphasis control (When AUX monitor bit in 0x0D byte is disabled) • 0: 0 dB • 1: 3.5 dB • 2: 6 dB • 3: 8.8 dB
0x08 Read/Write	DP Lane 1 TX/RX Control Register	7	b`0	Reserved
		6:4	b`000	DP Lane 1 Rx equalization gain control • 0: 0 dB • 1: 1.5 dB • 2: 3 dB • 3: 4.5 dB • 4: 6 dB • 5: 9 dB • 6: 12dB • 7: Reserved
		3:2	b`00	DP Lane 1 TX output swing control (When AUX monitor bit in 0x0D byte is disabled) • 0: 400 mVppd • 1: 600 mVppd • 2: 800 mVppd • 3: 1100 mVppd

Register offset	Register name	Bits	POR default value	Description
		1:0	b`00	DP Lane 1 pre-emphasis control (When AUX monitor bit in 0x0D byte is disabled) • 0: 0 dB • 1: 3.5 dB • 2: 6 dB • 3: 8.8 dB
0x09 Read/Write	DP Lane 2 TX/RX Control Register	7	b`0	Reserved
		6:4	b`000	DP Lane 2 Rx equalization gain control • 0: 0 dB • 1: 1.5 dB • 2: 3 dB • 3: 4.5 dB • 4: 6 dB • 5: 9 dB • 6: 12dB • 7: Reserved
		3:2	b`00	DP Lane 2 TX output swing control (When AUX monitor bit in 0x0D byte is disabled) • 0: 400 mVppd • 1: 600 mVppd • 2: 800 mVppd • 3: 1100 mVppd
		1:0	b`00	DP Lane 2 pre-emphasis control (When AUX monitor bit in 0x0D byte is disabled) • 0: 0 dB • 1: 3.5 dB • 2: 6 dB • 3: 8.8 dB
0x0A Read/Write	DP Lane 3 TX/RX Control Register	7	b`0	Reserved
		6:4	b`000	DP Lane 3 Rx equalization gain control • 0: 0 dB • 1: 1.5 dB • 2: 3 dB • 3: 4.5 dB • 4: 6 dB • 5: 9 dB • 6: 12 dB • 7: Reserved

Register offset	Register name	Bits	POR default value	Description
		3:2	b`00	DP Lane 3 TX output swing control (When AUX monitor bit in 0x0D byte is disabled) • 0: 400 mVppd • 1: 600 mVppd • 2: 800 mVppd • 3: 1100 mVppd
		1:0	b`00	DP Lane 3 pre-emphasis control (When AUX monitor bit in 0x0D byte is disabled) • 0: 0 dB • 1: 3.5 dB • 2: 6 dB • 3: 8.8 dB
0x0B Read/Write	Mode control 1	7:6	b`00	DFP or /UFP application mode • 0: DFP configuration, without external 4.7Ω resistors on the DRXn pins. This setting also applies to UFP_Dongle configuration. • 1: DFP configuration, with external 4.7Ω resistors on the DRXn pins for higher level surge protection • 2: UFP configuration. • 3: Reserved (DFP/UFP application mode must be set once before taking PTN36502/PTN36502A out of deep power saving state. Changing these bits after the operational mode of the device is set to a mode other than deep power saving state is not allowed)
		5	b`0	Plug orientation control. This orientation condition applies to both high speed TX/RX configuration and AUX crossbar switch. • 0: normal plug orientation of Type-C connection • 1: reverse plug orientation of Type-C connection
		4	b`0	AUX monitor polarity control. • 0: Polarity automatically controlled by plug orientation configuration • 1: reverse polarity with respect to automatically controlled polarity.
		3	b`0	AUX crossbar switch control • 0: AUX switch path disabled. (AUX switch is in high-Z state; but AUX monitor is still connected to DAUXP/N pins) • 1: AUX switch path enabled in DP mode

Register offset	Register name	Bits	POR default value	Description
		2:0	b`000	Operational mode of the device. Refer to 7.6.3 for mode transition requirement. • 0: Deep power saving state • 1: USB 3.1 Gen 1 only • 2: USB 3.1 Gen 1 and 2-lane DP • 3: 4-lane DP • 4-7: Reserved
0X0C Read/Write	Squelch threshold	7:4	b'0001	Upstream side (left) squelch threshold setting • 0: 75mVpp • 1: 80mVpp • 2: 90mVpp • 3: 100mVpp • Other values are reserved
		3:0	b'0001	Downstream side (right) squelch threshold setting • 0: 75mVpp • 1: 80mVpp • 2: 90mVpp • 3: 100mVpp • Other values are reserved
0x0D Read/Write	Device control	7	b`1	AUX monitoring function • 0: Disabled. DisplayPort OS/DE settings are adjusted through GPIO/ I^2C registers. • 1: Enabled. DisplayPort OS/DE settings are adjusted autonomously by monitoring AUX channel traffic.
		6:1	b`000000	Reserved
		0	b`0	Device Reset bit. This is a self-clearing bit, and reading this register will always return 0. • Writing a '1' to this register will soft reset the device including I^2C register contents and internal digital logics, while the chip continuing to operating under I^2C mode. • Writing a '0' does not have any effect.
0x0E-0x1F	Reserved			Reserved for NXP Internal use only; Do not write to these registers
0x20-0xFF	Reserved			Reserved for NXP Internal use only; Do not write to these registers

7.6.7 I^2C read/write operations

PTN36502/PTN36502A has an I^2C register interface that enables system integrator to program register settings suitable as per application needs. Table 18 describes possible

settings for different functions of the device. Though the device can be pin configured through board-strapping or it also allows the system integrator to override those settings by programming the registers through I^2C. I^2C–bus can support up to 1 MHz data rate, and 8-bit device slave address is defined in Table 19.

Table 19. Read/write device slave address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTN36502 slave address	8	0	0	1	1	0	1	0	R/W
PTN36502A slave address	8	0	0	1	0	0	1	0	R/W

PTN36502/PTN36502A supports programming of the registers through the I^2C interface. Reading/writing the registers must be done according to the following sequences.

The read sequence contains two phases:

- Command phase
- Data phase

The command phase is an I^2C write to PTN36502/PTN36502A that contains a single data byte. The LS bit indicates if the command that is being executed will read or write data from/to the device. The other 7 bits are the device slave address. The single data byte followed is the register offset that is used to indicate which register address is being accessed (read or written). The data phase is a second I^2C transaction that starts with 7-bit slave address, with LS bit set to 1 indicating a read operation, followed by a 8-bit data read back from the device register address.

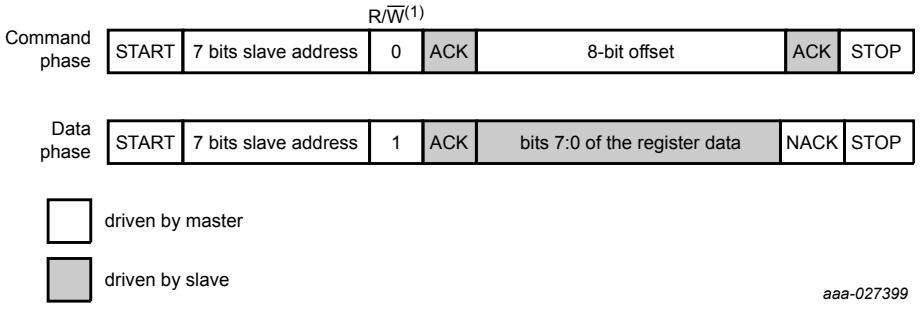


Figure 11. I^2C read sequence

(1) R/$\overline{W}$ = read/write bit. 0b = I^2C write; 1b = I^2C read

The write sequence starts with 7-bit slave address, with LS bit set to 0 indicating a write access. The next byte is the register offset that is used to indicate which device register address is being written to. The last byte is the 8-bit register data that will be written to the device register address.

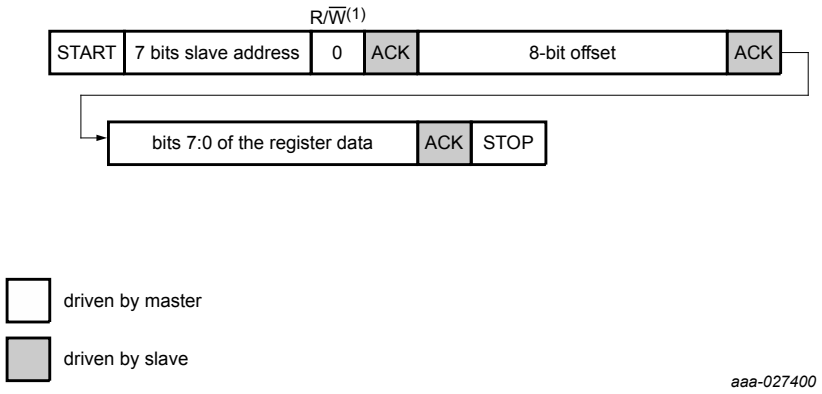


Figure 12. I^2C write sequence

(1) R/$\overline{W}$ = read/write bit. 0b = I^2C write; 1b = I^2C read

8 Limiting values

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}[1]	Supply voltage		-0.5	+2.5	V
VI[1]	Input voltage	EN, SCL/C1, SDA/C2	-0.5	4.0	V
		High speed pins	-0.5	2.5	V
		AUX pins	-0.5	7	V
T_{stg}	Storage temperature		-65	150	°C
V_{esd}	Electro Static Discharge	HBM[2] for High speed and AUX pins	-	8000	V
		HBM for control pins		4000	V
		CDM[3] for High speed and AUX pins	-	1000	V
		CDM for control pins		500	V
Surge Tolerance	IEC61000-4-5 8/20 µs capable source with 2Ω source series impedance	DRX1P/N and DRX2P/N pins and DAUXP/N pins with 4.7 Ohm series resistors			
		Positive surge pulse		+16	V
		Negative surge pulse	-16		V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.
[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.
[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA

9 Recommended operating conditions

Table 21. Recommended operating conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.8 V Supply option	1.7	1.8	1.9	V
V_I	Input voltage	Control and configuration pins (EN, SCL/C1, SDA/C2) in GPIO mode	-0.3	VDD1V8	VDD1V8+0.3	V
		Control and configuration pins (EN, SCL/C1, SDA/C2) in I^2C mode	-0.3		+3.6	V
		High speed Data pins	-0.3		VDD1V8+0.3	V
		AUX pins	-0.3		4	V
T_{amb}	Ambient temperature	Operating in free air	-40	-	85	°C

10 Characteristics

10.1 Device characteristics

Table 22. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{Startup}$	Start-up time	Between supply voltage exceeding 1.1V until sampling of the EN/C1/C2 pin	-		1.5	ms
T_{VDD_rampup}	Supply voltage ramp-up time	Between 0V and 1.5V	-		3.7	ms
$t_{Startup\_USB}$	USB start-up time	Time between configuration in USB operating mode until automatic receive detection is active.	-		7	ms
$t_{S(EN-DIS)}$	Enable to Disable settling time (Deep power saving mode)	Power down control change until deep power saving mode. Device is supplied with valid supply voltage	-		1	ms
t_{rcfg}	Reconfiguration time	Any configuration pin change (from one setting to another setting) to specified operating characteristics. Device is supplied with valid supply voltage. This includes control pin changes	-		0.2	ms
t_{PD}	Differential Propagation Delay	Differential propagation delay between 50% level at input and output			0.6	ns
t_{idle}	Idle Time	Time to wait before getting into power saving U2/U3 state (in USB mode)		300	400	ms
$t_{ps-exit}$	Power Saving Exit Time	Time for exiting from Power saving U2/U3 state and get into Active state (in USB mode see Figure 15)			115	µs
$t_{hold-port}$ t_{hold1}	Hold time for data on C1/C2 pin after VDD ramps up	hold time for determining port role - DFP or UFP	1.5			ms
$t_{hold-mode}$ t_{hold2}	Hold time for data on C1/C2 pin after EN goes 0→1	hold time for definition of mode of operation	100		2000	µs
t_{setup3}	Setup time for EN=HiZ and data on C1/C2 pins before EN goes HiZ→1	setup time for mode re-configuration	150			µs
t_{hold3}	Hold time for data on C1/C2 pin after EN goes HiZ→1	hold time for mode re-configuration	100		2000	µs
t_{hold4}	Hold time for channel condition data on C1/C2 pin after EN goes 1→HiZ	hold time for channel condition before mode re-configuration	20			µs
$T_{d\ (act-idle)}$	Delay time from active to idle	Reaction time for squelch detection circuit		6	21	ns
$T_{d\ (idle-act)}$	Delay time from idle to active	Reaction time for squelch detection circuit		4	20	ns
$Rth_{(j-a)}$	Thermal resistance from junction to ambient	JEDEC still air test environment		55		°C/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active state (Mode 1 USB 3.1 Gen 1 only) TX Output Swing 1000 mVppd TX De-emphasis is -3.5dB RX Equalization gain 6 dB		115		mA
		Active state (Mode 2, 2-lane DP and USB 3.1 Gen 1) DP TX Output Swing 600mV DP TX Pre-emphasis 3.5 dB USB TX Output Swing 1000 mVppd USB TX De-emphasis is -3.5 dB RX Equalization gain 6 dB		225		mA
		Active state (Mode 3, 4-lane DP) TX Output Swing 600 mVppd TX Pre-emphasis is 3.5 dB RX Equalization gain 6 dB		220		mA
		U2/U3 Power Saving states (USB mode)		1.16	1.70	mA
		No USB connection state (Rx termination detection active)		0.77	0.96	mA
		DP 4-lane @ HBR2 level 0 TX output Swing 400 mVppd TX Pre-emphasis is 0 dB RX Equalization is 6 dB AUX and I^2C Idle		150		mA
		DP 2-lane @ HBR2 level 0 TX output Swing 400 mVppd TX Pre-emphasis is 0 dB RX Equalization is 6 dB AUX and I^2C Idle		75		mA
		DP 1-lane @ HBR2 level 0 TX output Swing 400 mVppd TX Pre-emphasis is 0 dB RX Equalization is 6 dB AUX and I^2C Idle		38		mA
		DP 4-lane D3 state, with AUX switch and AUX monitoring enabled		0.5	0.66	mA
		Deep Power-saving state		3		µA
DDNEXT1	Near end cross talk for adjacent high speed differential pins (between TX and RX signal pairs within the same USB 3.1 Gen 1 port)	@ 2.7 GHz between DTX1 and DRX1; Between DTX2 and DRX2; Between B_IO and A_IN; Between D_IO and C_IN	-45			dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDNEXT2	Near end cross talk for adjacent high speed differential pins	@ 2.7 GHz between DTX1 and DRX2; Between DTX2 and DRX1; Between B_IO and C_IN Between D_IO and A_IN	-45			dB
$Xtak_{OO}$	The crosstalk between two output drivers for far end crosstalk analysis. (between any two DP signal pairs)	@2.7 GHz Between any two channels among DRX1, DRX2, DTX1 and DTX2.	-35			dB

10.2 USB 3.1 Gen 1 receiver dynamic characteristics

Table 23. USB 3.1 Gen 1 receiver dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{RX-DC}	RX DC common mode impedance		18		30	Ω
$R_{RX-DIFF-DC}$	DC Differential Impedance		72		120	Ω
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input High Impedance	DC common-mode input impedance when output of redriver is not terminated and VDD between 1.7 and 1.9V. USB3.x controller should stop doing RX Detection before VDD is powered down to avoid detection of low-ohmic RX input termination	25			KΩ
$V_{RX-DIFF-PP}$	Rx Differential Input voltage (peak to peak)		100		1200	mVpp
$V_{squelch-DIFF-PP}$	Squelch threshold level	Default value from I^2C 0X0C byte		80		mVppd
$V_{RX-DC-CM}$	RX Common mode DC voltage			1.8		V
$V_{RX-CM-AC-P}$	RX AC Common Mode Voltage tolerance				150	mVpp
$RL_{DD11,RX}$	Rx Differential mode Return Loss at upstream (left) side of PTN36502/ PTN36502A	10 MHz to 1250 MHz		14		dB
		1250 MHz to 2500 MHz		9		dB
		2500 MHz to 3000 MHz		8		dB
		3000 MHz to 5400MHz		6		dB
	Rx Differential mode Return Loss at downstream (right) side of PTN36 502/PTN36502A	10 MHz to 1250 MHz		14		dB
		1250 MHz to 2500 MHz		11		dB
		2500 MHz to 3000 MHz		11		dB
		3000 MHz to 5400MHz		11		dB
$RL_{CC11,RX}$	Rx Common mode Return Loss at upstream (left) side of PTN36502/ PTN36502A	10 MHz to 1250 MHz		15		dB
		1250 MHz to 2500 MHz		11		dB
		2500 MHz to 3000 MHz		10		dB
		3000 MHz to 5400 MHz		7		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Rx Common mode Return Loss at downstream (right) side of PTN36502/PTN36502A	10 MHz to 1250 MHz		16		dB
		1250 MHz to 2500 MHz		13		dB
		2500 MHz to 3000 MHz		13		dB
		3000 MHz to 5400MHz		12		dB

10.3 USB 3.1 Gen 1 transmitter dynamic characteristics

Table 24. USB 3.1 Gen 1 transmitter dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{TX-DC}	TX DC common mode Impedance		18		30	Ω
$R_{TX-DIFF-DC}$	TX Differential Impedance		72		120	Ω
$V_{TX-DIFF-PP}$	TX Differential Output voltage (peak to peak)	R_{load} = 100 Ω OS = 900 mV	770	900	1050	mVpp
$V_{TX-DIFF-PP}$	TX Differential Output voltage (peak to peak)	R_{load} = 100 Ω OS = 1000 mV	855	1000	1150	mVpp
$V_{TX-DIFF-PP}$	TX Differential Output voltage (peak to peak)	R_{load} = 100 Ω OS = 1100 mV	940	1100	1250	mVpp
$V_{TX-DC-CM}$	TX DC common mode output voltage	OS = 1000 mV VDD = 1.8 V		1.3		V
$V_{TX-CM-AC-PP\_ACTIVE}$	TX AC Common mode output voltage in active state	Device input fed with differential signal			100	mVpp
$V_{TX-IDLE-DIFF-AC-pp}$	TX AC differential output voltage	When link is in electrical idle			10	mVpp
V_{DETECT}	Voltage change allowed during receiver detection	Positive voltage swing to sense the receiver termination detection			600	mV
T_{TXR}	TX rise time	Measured using 20% and 80% levels	50	60	80	ps
T_{TXF}	TX fall time	Measured using 20% and 80% levels	50	60	80	ps
$T_{TX-RF-MIS}$	TX Rise/Fall time mismatch	Measured using 20% and 80% levels			20	ps
$RL_{DD11,TX}$	TX Differential mode Return Loss at upstream (left) side of PTN36502/PTN36502A	10 MHz to 1250 MHz		14		dB
		1250 MHz to 2500 MHz		11		dB
		2500 MHz to 3000 MHz		11		dB
		3000 MHz to 5400 MHz		11		dB
	TX Differential mode Return Loss at downstream (right) side of PTN36502/PTN36502A	10 MHz to 1250 MHz		14		dB
		1250 MHz to 2500 MHz		11		dB
		2500 MHz to 3000 MHz		11		dB
		3000 MHz to 5400 MHz		9		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$RL_{CC11,TX}$	TX Common Mode Return Loss at upstream (left) side of PTN36502/ PTN36502A	10 MHz to 1250 MHz		17		dB
		1250 MHz to 2500 MHz		14		dB
		2500 MHz to 3000 MHz		14		dB
		3000 MHz to 5400 MHz		14		dB
	TX Common Mode Return Loss at downstream (right) side of PTN3650 2/PTN36502A	10 MHz to 1250 MHz		16		dB
		1250 MHz to 2500 MHz		14		dB
		2500 MHz to 3000 MHz		14		dB
		3000 MHz to 5400 MHz		10		dB

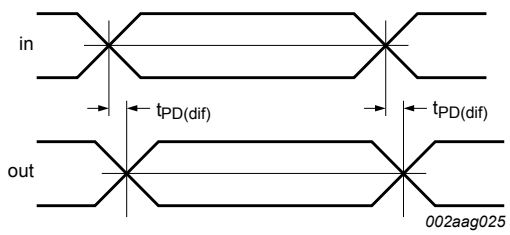


Figure 13. Propagation delay

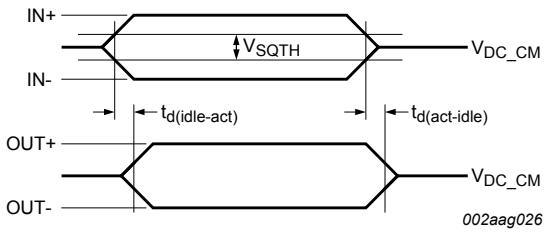


Figure 14. LFPS electrical idle transitions in U0/U1 mode

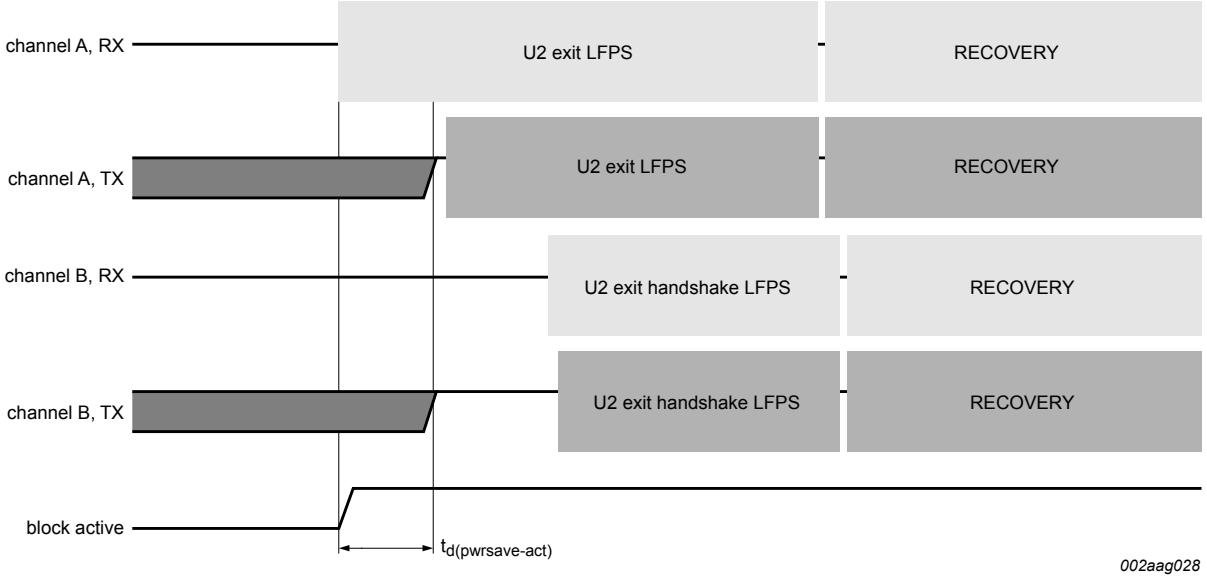


Figure 15. U2/U3 exit behavior

10.4 USB jitter characteristics

Table 25. USB jitter characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TJ_{TX} [1][2]	Total Jitter at test point C	Total jitter at test point C		0.19		UI_{PP}[3]
DJ_{TX} [1]	Deterministic jitter	Total jitter at test point C		0.11		UI_{PP}[3]
RJ_{TX} [1][2]	Random Jitter	Total jitter at test point C		0.08		UI_{PP}[3]

[1] Measured at Test Point C with 5Gbps K28.5 pattern, 1000mVpp source amplitude, -3.5dB source de-emphasis and 9dB RX-EQ setting
[2] RJ(peak to peak(pp)) is calculated as 14.069 times the RMS random jitter for 10-12 bit error rate
[3] UI=200ps

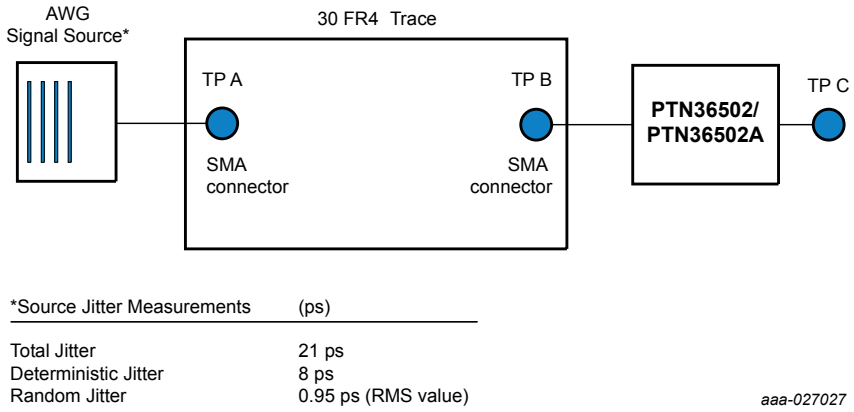


Figure 16. Jitter measurement setup

10.5 DisplayPort receiver dynamic characteristics

Table 26. DisplayPort receiver dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{RX-DIFF-DC}$	Differential input Impedance		72		120	Ω
$V_{squelch-DIFF-PP}$	Squelch threshold level	Default value from I^2C 0X0C byte		80		mVpp
$V_{RX-DIFF-PP}$	Rx Differential Input voltage (peak to peak)	HBR, HBR2	100		1200	mVppd
		RBR (When $V_{squelch-DIFF-PP}$ = 80 mV)	80		1200	mVppd
$V_{RX-DC-CM}$	RX DC common mode voltage		0		2	V
$V_{RX-CM-AC-P}$	RX AC Common Mode Voltage tolerance				150	mVpp
$RL_{DD11,RX}$	Rx Differential mode Return Loss	10 MHz-1250 MHz		14		dB
		1250 MHz-2500 MHz		9		dB
		2500 MHz-3000 MHz		8		dB
		3000 MHz-5400MHz		6		dB
$RL_{CC11,RX}$	Rx Common mode Return Loss	10 MHz-1250 MHz		15		dB
		1250 MHz-2500 MHz		11		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		2500 MHz-3000 MHz		10		dB
		3000 MHz-5400 MHz		7		dB
$RXEQ_{AC, Gain}$	AC Receive Equalization gain @ Nyquist freq. w.r.t DC gain	I^2C setting or appropriate GPIO pin setting				
		I^2C setting = 1 (1.5dB)		1.5		dB
		I^2C setting = 2 (3.0dB) C1/C2 setting=LOW		3		dB
		I^2C setting = 3 (4.5dB)		4.5		dB
		I^2C setting = 4 (6.0dB) C1/C2 setting = OPEN		6		dB
		I^2C setting = 5 (9.0dB) C1/C2 setting = HIGH		9		dB
		I^2C setting = 6 (12.0dB)		12		dB

10.6 DisplayPort transmitter dynamic characteristics

Table 27. DisplayPort transmitter dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{TX-DC}	TX DC common mode Impedance		18		30	Ω
$R_{TX-DIFF-DC}$	TX Differential Impedance		72		120	Ω
$V_{TX-DIFF-PP}$	TX Differential Output voltage (peak to peak)	R_{load} = 100 Ω I^2C setting = 0 (400 mV)	340	400	470	mVpp
		R_{load} = 100 Ω I^2C setting = 1 (600 mV)	510	600	700	mVpp
		R_{load} = 100 Ω I^2C setting = 2 (800 mV)	690	800	930	mVpp
		R_{load} = 100 Ω I^2C setting = 3 (1100 mV)	900	1100	1250	mVpp
$V_{TX-PREEMPRATIO}$	Transmit pre-emphasis in DP mode; values for OS=400mV.	I^2C setting = 0 (0 dB)	0	0	0	dB
		I^2C setting = 1 (3.5 dB)	2.6	3.5	4	dB
		I^2C setting = 2 (6.0 dB)	4.8	6	7	dB
		I^2C setting = 3 (8.8 dB)	7.3	8.8	10	dB
$V_{TX-DC-CM}$	TX DC common mode output voltage	OS = 1100 mV VDD = 1.8 V		1.25		V
$V_{TX-CM-AC-RMS\_ACTIVE}$	TX AC Common mode RMS output voltage in active state. Measured using 8b10b valid pattern with 50% transition density. Measured at supported frequencies within the frequency tolerance range. Time domain measurement.	RBR, HBR			20	mVrms
		HBR2			30	mVrms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TX-IDLE-DIFF-AC-pp}$	TX AC differential output voltage	When link is in electrical idle			10	mVpp
T_{TXR}	TX rise time	Measured using 20% and 80% levels	50	60	80	ps
T_{TXF}	TX fall time	Measured using 20% and 80% levels	50	60	80	ps
$T_{TX-RF-MIS}$	TX Rise/Fall time mismatch	Measured using 20% and 80% levels			20	ps
$RL_{DD11,TX}$	TX Differential mode Return Loss	10 MHz-1250 MHz		14		dB
		1250 MHz-2500 MHz		11		dB
		2500 MHz-3000 MHz		11		dB
		3000 MHz-5400 MHz		9		dB
$RL_{CC11,TX}$	TX Common mode Return Loss	10 MHz-1250 MHz		16		dB
		1250 MHz-2500 MHz		14		dB
		2500 MHz-3000 MHz		14		dB
		3000 MHz-5400 MHz		10		dB
$I_{TX-SHORT}$	TX Short circuit current limit	Total drive current of the transmitter when it is shorted to its ground			50	mA

10.7 AUX switch and AUX monitor characteristics

Table 28. AUX switch and AUX monitor characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
Vi-dc	Bias Voltage at the pin	UAUXP/N & DAUXP/N pins	0		3.6	V
r_{AUX}	AUX bit rate			1		Mbps
VAUX-AC-DIFF-pp	AUX AC differential peak-to-peak voltage	UAUXP/N & DAUXP/N pins	0.27		1.38	Vppd
I_{IL}	Leakage current at the pin	VDD= 1.8V; Pin voltage 3.6V In deep power saving mode			+1	µA
I_{bck}	Back current sunk from pin to powered down supply	VDD=0, Pin voltage = 3.6V			+1	µA
Zin	AUX monitor differential input impedance	Over frequency range of interest DC to 50 MHz		1M		Ω
Cin	AUX monitor AC coupling capacitance			10		pF
Ron	ON-state resistance	DC voltage = 0 to 3.6V, I = 20 mA		3.3	5.6	Ω
		DC voltage = 0 to 0.6V, I = 20 mA		3	4.0	Ω
		DC voltage = 3.0 to 3.6V, I = 20 mA		3.3	5.6	Ω
Imax	Maximum sustained DC current flow				20	mA

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
T_{AUX_OFF}	Switching time to turn off AUX switch	AUX reaction time from DP to USB mode		29	39	µs
T_{AUX_ON}	Switching time to turn on AUX switch	AUX reaction time from USB to DP mode		29	39	µs
t_{pd}	Propagation delay	DC voltage= 0 to 3.6V, I=20mA		174	198	ps
		DC voltage= 0 to 0.6V, I=20mA		144	156	ps
		DC voltage= 3.0 to 3.6V, I=20mA		174	198	ps
t_{SK}	Intra pair skew			30	47	ps
BW	-3 dB bandwidth			100		MHz

[1] All S-parameter measurements are with respect to 100 Ω differential impedance reference and 50 Ω single-ended impedance reference.

10.8 Ternary control characteristics

Table 29. Ternary control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	Input leakage current	Measured with input at V_{IH} =VDD or V_{IL} = 0; VDD = 1.8V	-6.25		6.25	µA
I_{LM}	Input leakage current	Measured with input between $V_{IM\ (min)}$ and $V_{IM\ (max)}$			2	µA
V_{IH}	High level voltage		0.75*VDD		VDD+0.3	V
V_{IM}	Voltage at unconnected/ open condition		0.375*VDD		0.625*VDD	V
V_{IL}	Low level voltage				0.25*VDD	V
I_{IL}	Leakage current at the pin	VDD= 1.8V; Pin voltage 2.2V			+1	µA
I_{bck}	Back current sunk from pin to powered down supply	Pin voltage = 2.2V			+1	µA
R_{pu}	Internal Pull-up resistance	Ternary setting		500		kΩ
R_{pd}	Internal Pull-down resistance	Ternary setting		500		kΩ
C_{pin}	Maximum allowed capacitance at the pin				100	pF

10.9 I^2C dynamic characteristics

Table 30. I^2C dynamic characteristics

Applicable across operating temperature and power supply ranges as Recommended operating conditions (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{I2C}	I^2C Clock frequency		0		1000	kHz
V_{IH}	HIGH-level Input voltage		1.19			V
V_{IL}	LOW-level Input voltage				0.57	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}	Hysteresis of Schmitt trigger inputs	V_{pullup} < 3.6V	0.095			V
V_{OL}	LOW-level output voltage at 3mA sink current	V_{pullup} < 3.6V	0		0.4	V
I_{OL}	LOW-level output current	V_{OL} =0.4V; Standard and Fast modes	3			mA
		V_{OL} =0.4V; Fast mode plus	20			mA
		V_{OL} =0.6V; Fast mode	6			mA
I_{IL}	LOW-level input current	Pin voltage = 0.1* V_{pullup} to 0.9*$V_{pullup, max}$	-10		10	µA
C_I	Capacitance of IO pin				10	pF
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26			µs
t_{LOW}	LOW period of I^2C clock	Fast mode plus	0.5			µs
t_{HIGH}	HIGH period of I^2C clock	Fast mode plus	0.26			µs
$T_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26			µs
$T_{HD,DAT}$	Data Hold time	Fast mode plus	0			µs
$T_{SU,DAT}$	Data Setup time	Fast mode plus	50			ns
T_r	Rise time of I2C_SCL and I2C_SDA signals	Fast mode plus	-		120	ns
T_f	Fall time of I2C_SCL and I2C_SDA signals	Fast mode plus	-		120	ns
$T_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26			µs
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5			µs
$t_{VD,DAT}$	Data valid time	Fast mode plus			0.45	µs
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus			0.45	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter		0		50	ns

Note: *V_{pullup} is external pull up voltage on SCL and SDA pins. The voltage can be up to 3.6V from another power supply.*

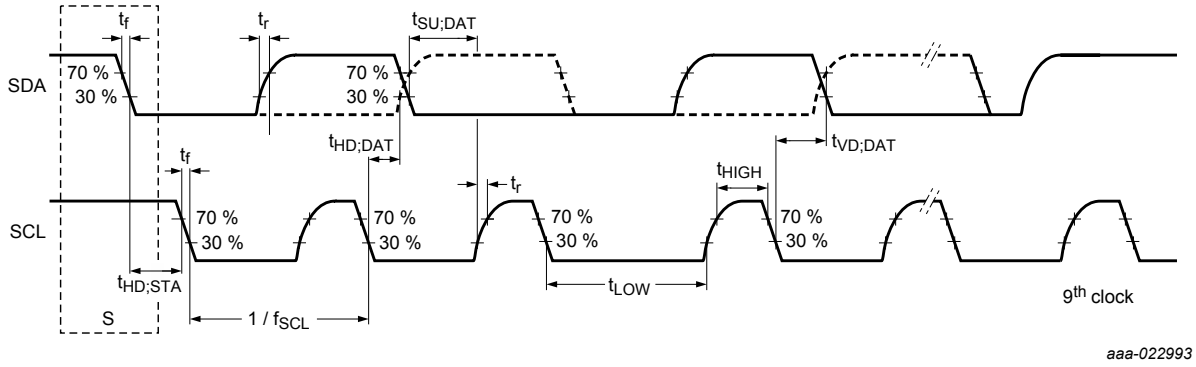


Figure 17. I^2C-bus timing diagram

11 Package summary

Terminal position code: Q (quad)

Package type descriptive code: HX2QFN24

Package style descriptive code: HXQFN (thermal enhanced extremely thin quad flatpack; no leads)

Package body material type: P (plastic)

Mounting method type: S (surface mount)

Issue date: 16-12-2016

Manufacturer package code: SOT1903-1

Table 31. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.35	2.4	2.45	mm
package width	3.15	3.2	3.25	mm
seated height	0.3	0.35	0.4	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	24	-	A/A

12 Package outline

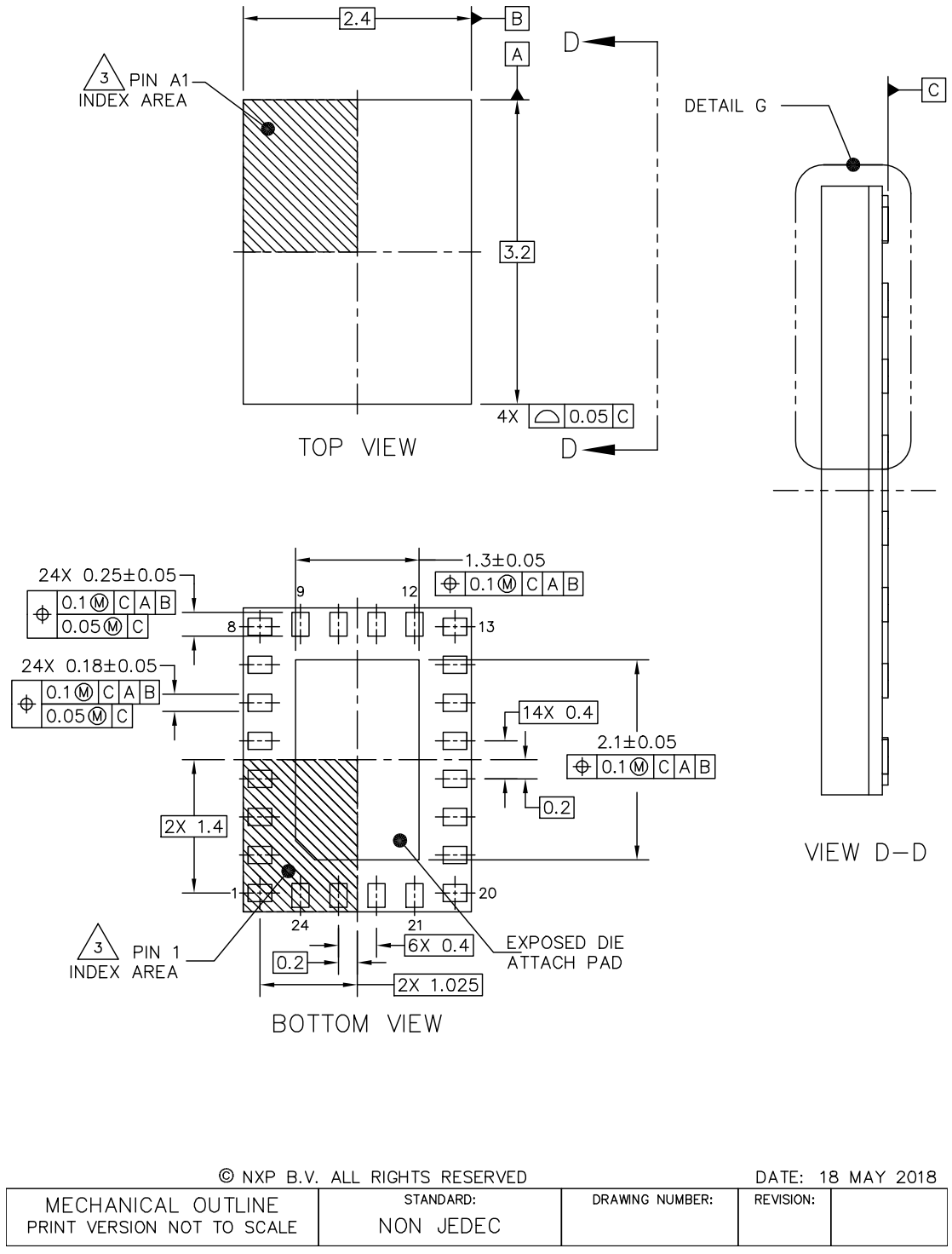
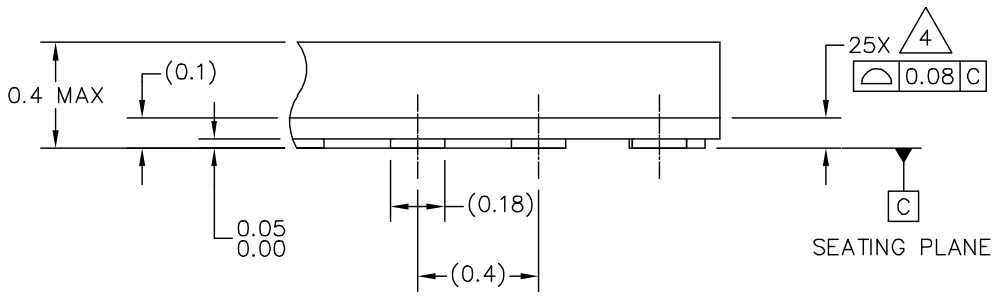


Figure 18. Package outline SOT1903-1



DETAIL G
VIEW ROTATED 90° CW

DATE: 18 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER:	REVISION:	

Figure 19. Package outline detail G of HX2QFN24 (SOT1903-1)

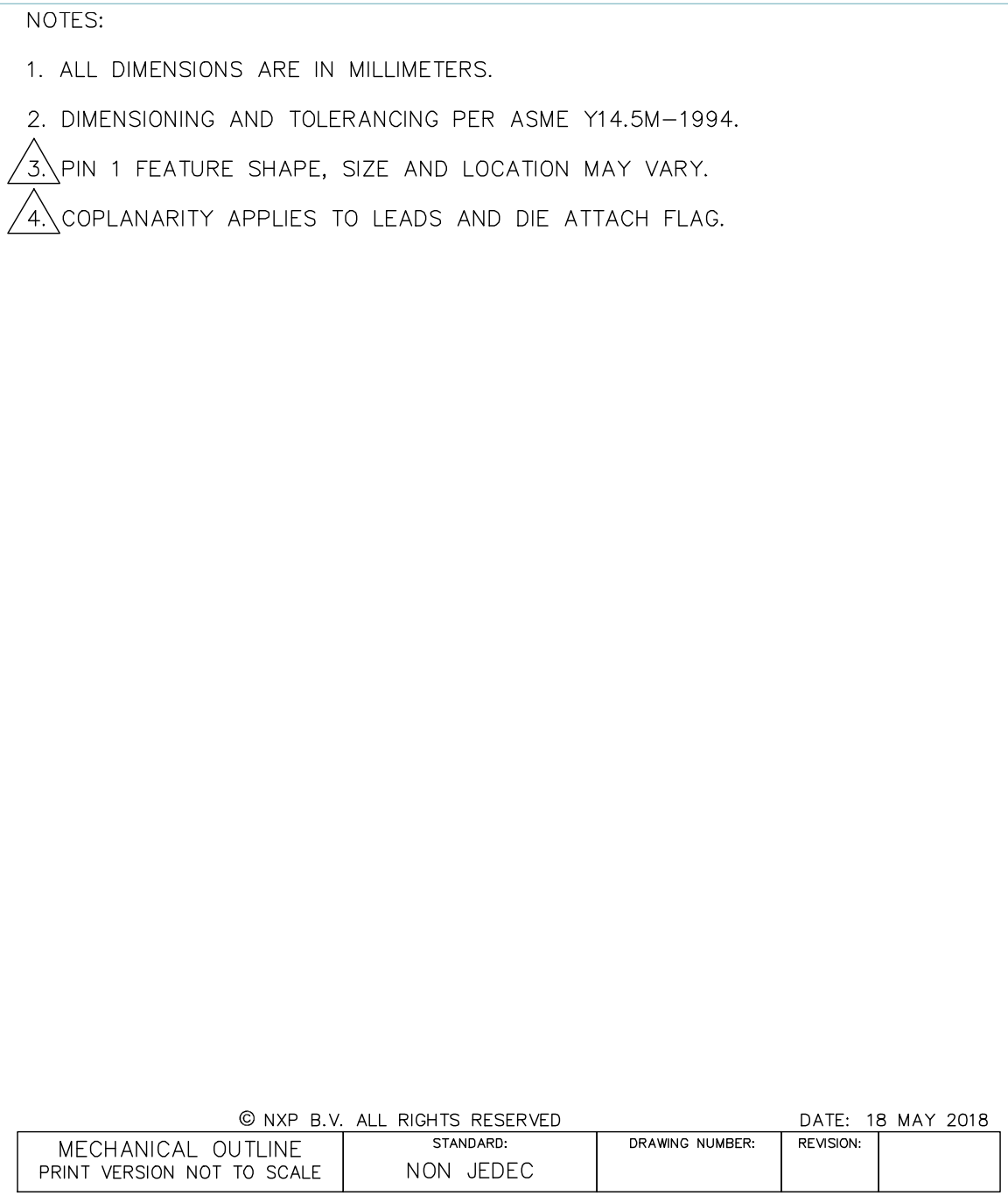
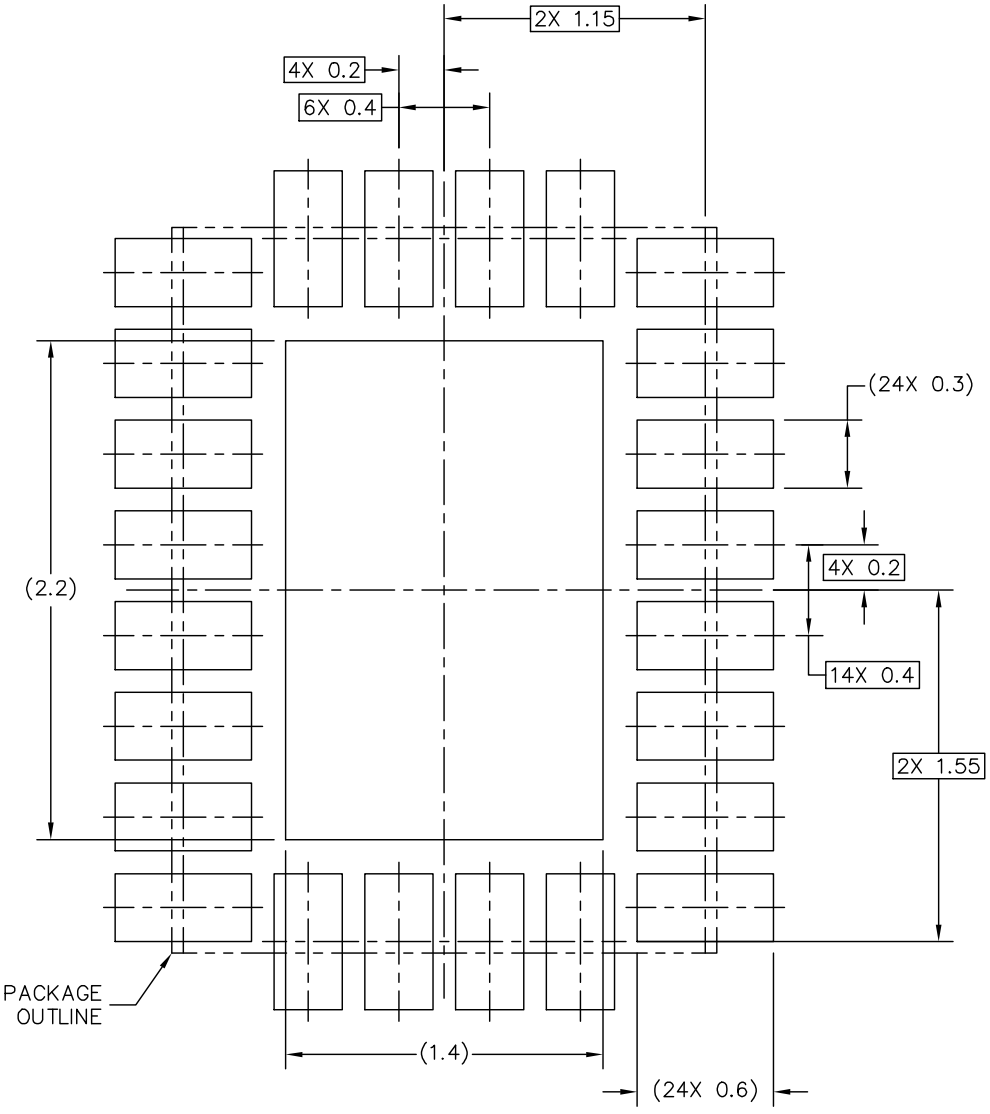


Figure 20. Package outline note HX2QFN24 (SOT1903-1)

13 Soldering



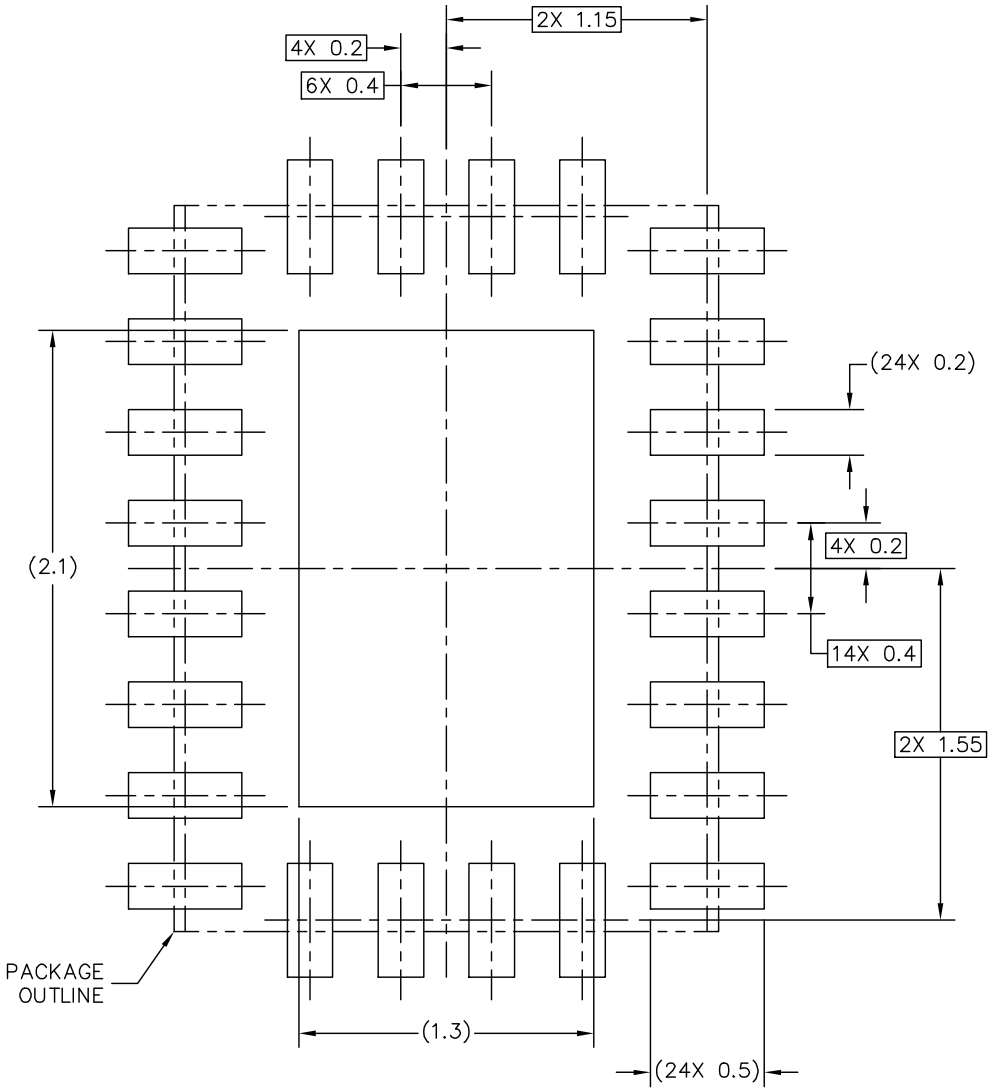
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 18 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER:	REVISION:	

Figure 21. Reflow soldering footprint for SOT1903-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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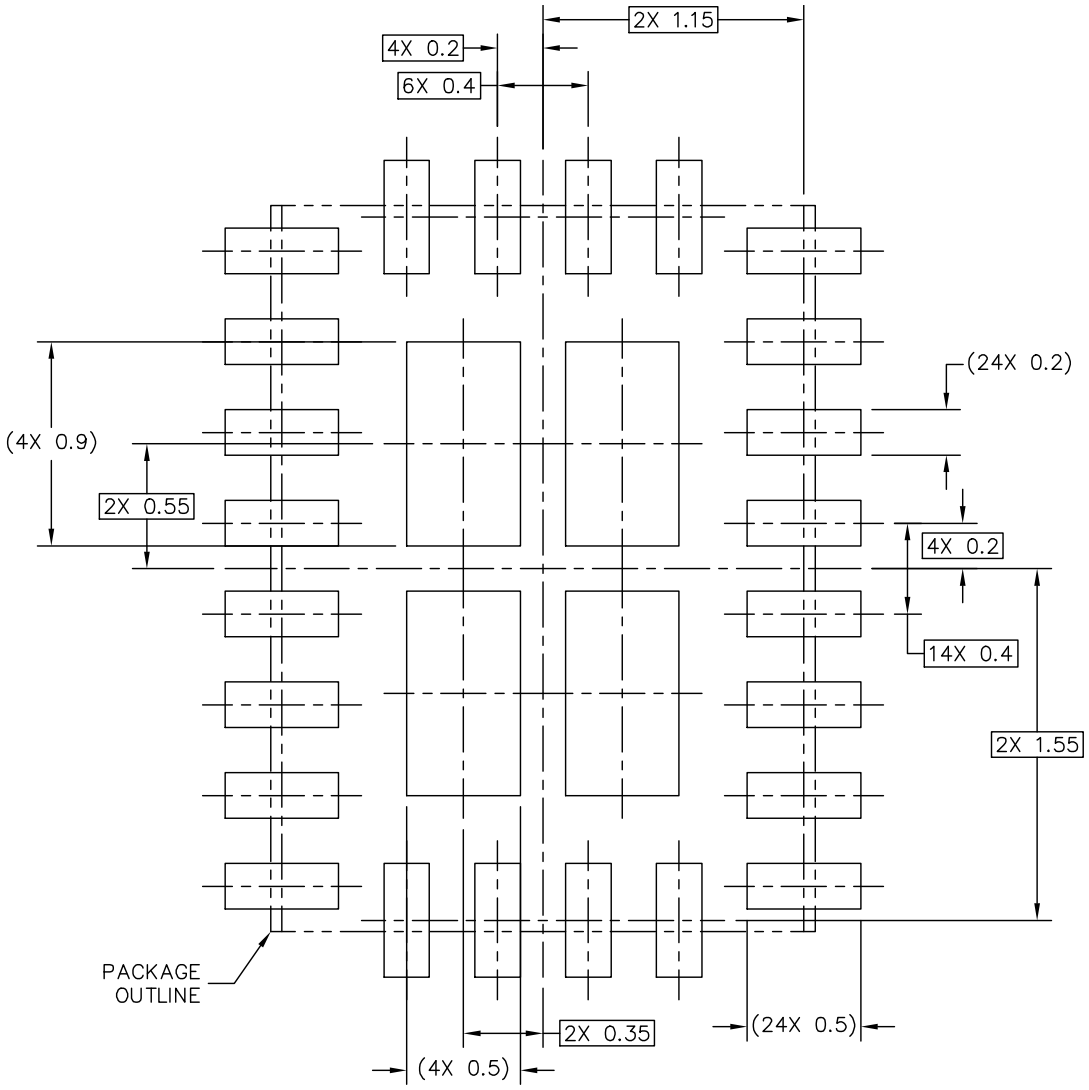
DATE: 18 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER:	REVISION:	

Figure 22. Reflow soldering footprint part2 for HX2QFN24 (SOT1903-1)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 18 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER:	REVISION:	

Figure 23. Reflow soldering footprint part3 for HX2QFN24 (SOT1903-1)

14 Packing information

SOT1903-1 (HX2QFN24); Reel pack, SMD, 7" Q1 standard product orientation; Ordering code (12NC) ending 115

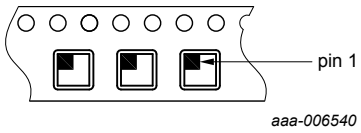
14.1 Dimensions and quantities

Table 32. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs)	Reels per box
178 × 12	3000	1

[1] d = reel diameter; w = tape width.

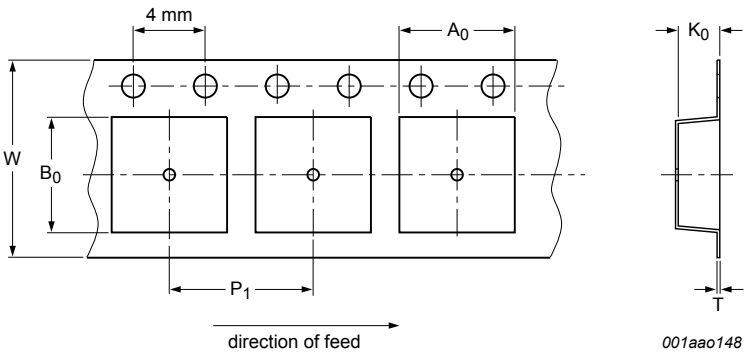
14.2 Product orientation



Pin 1 is in quadrant Q1/T1.

Figure 24. Product orientation in carrier tape

14.3 Carrier tape dimensions



Not drawn to scale.

Figure 25. Carrier tape dimensions

Table 33. Carrier tape dimensions

In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.60 ± 0.05	3.40 ± 0.05	0.53 ± 0.05	0.25 ± 0.03	8 ± 0.1	12+0.3/-0.1

15 Abbreviations

Table 34. Abbreviations

Acronym	Description
AIO	All in One Computer platform
CDM	Charged Device Model
DFP	Downstream Facing Port
DP	DisplayPort
Gbps	Giga bits per second
HBM	Human Body Model
LFPS	Low Frequency Periodic Signaling
LPM	Link Power Management
NC	No Connect
Rx	Receiver
SI	Signal Integrity
TX	Transmitter
UFP	Upstream Facing Port
USB	Universal Serial Bus

16 Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN36502_PTN36502A v.3.0	20180928	Product data sheet	-	PTN36502 v.2.0
Modifications	• Added part type PTN36502A			
PTN36502 v.2.0	20180614	Product data sheet	-	PTN36502 v.1.0
Modifications	• Added Section 11 • Section 12 and Section 13: added min/max dimensions, no change to device • Minor text edits • Updated Figure 3, Figure 4, and Figure 5			
PTN36502 v.1.0	20180316	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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