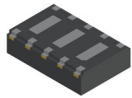


MECHANICAL CASE OUTLINE

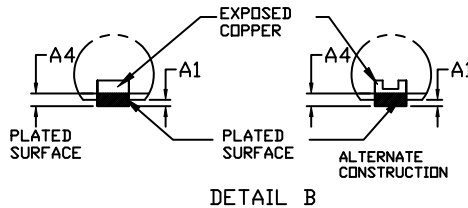
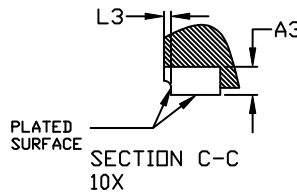
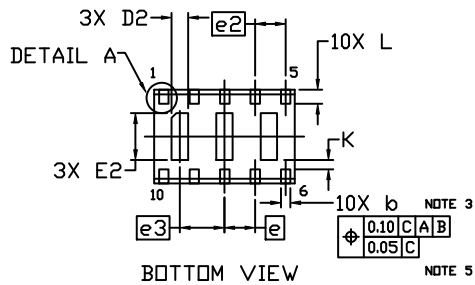
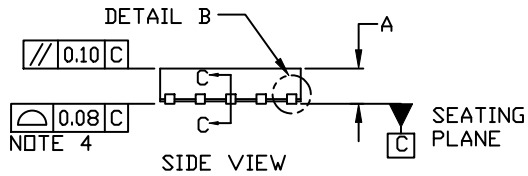
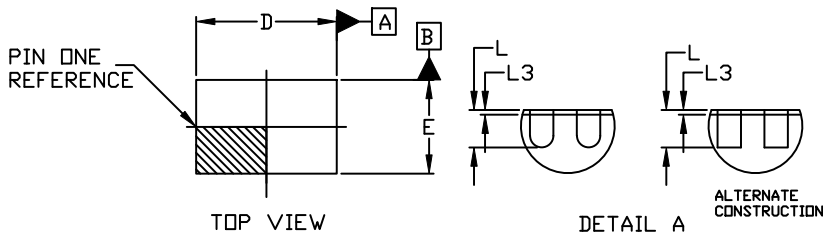
PACKAGE DIMENSIONS

ON Semiconductor®



WDFNW10 3.0x2.0, 0.65P CASE 515AL ISSUE B

DATE 05 FEB 2020

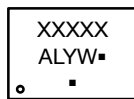


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
<i>b</i>	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	0.25	0.35	0.45
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
<i>e</i>	0.65 BSC		
<i>e2</i>	0.60 BSC		
<i>e3</i>	0.95 BSC		
K	0.20 REF		
L	0.25	0.30	0.35
L3	---	---	0.09

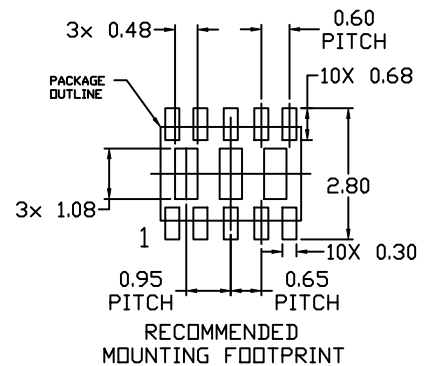
GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SLD16694.

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DESCRIPTION:	WDFNW10 3.0x2.0, 0.65P	PAGE 1 OF 1

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