AN-279
APPLICATION NOTE

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Using the AD650 Voltage to Frequency Converter as a Frequency to Voltage Converter

by Steve Martin

INTRODUCTION

The AD650 is a versatile, monolithic voltage to frequency converter (VFC) that utilizes a charge balanced architecture to obtain high performance in many applications. Like other charge balanced VFCs, the AD650 can be used in a reverse mode as a frequency to voltage converter (FVC). This application note discusses the FVC architecture and operation, component selection, a design example, and the fundamental trade-off between output ripple and circuit response time.

FVC CIRCUIT ARCHITECTURE

Figure 1 shows the major components of the FVC. The FVC includes a comparator, a one shot with a switch, a constant current source, and a lossy integrator. When the input signal crosses the threshold at the comparator input, the comparator triggers the one shot.

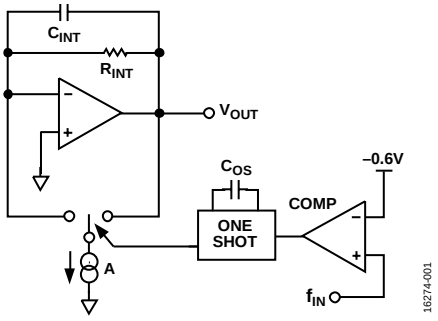

Figure 1. FVC Circuit Architecture

The one shot controls a single-pole, double throw switch that directs the current source to either the summing junction or the output of the lossy integrator. When the one shot is in the on state, a current is injected into the input of the integrator and the output of the one shot rises. When the one shot period has passed, the current is steered to the output of the integrator. Because the output is a low impedance node, the current has no effect on the circuit and is effectively turned off. During this time, the output falls due to the discharge of the integration capacitor (C_{INT}) through the integration resistor (R_{INT}). When constant triggering is applied to the comparator, the integration capacitor charges to a relatively steady value and is maintained by constant charging and discharging. The charge stored on C_{INT} is unaffected by loading because of the low output impedance of the op amp.

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10/2018—Rev. B to Rev. C

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9/2000—Rev. A to Rev. B

CIRCUIT OPERATION

Figure 2 shows a simplified schematic of the AD650 in the FVC mode. Figure 3 represents the current I(t) delivered to the lossy integrator. The current can be thought of as a series of charge packets delivered at input frequency (f_{IN}) = 1/t with current amplitude (α) and duration (t_{OS}).

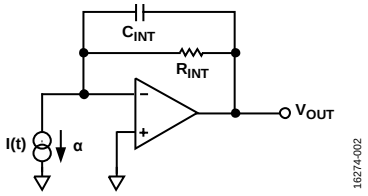

Figure 2. Simplified Schematic of the AD650 in FVC Mode

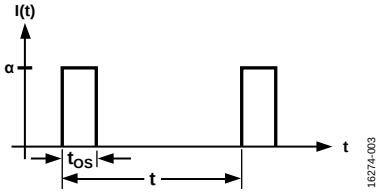

Figure 3. Current I(t) into Lossy Integrator

As Figure 3 indicates, determine the average input current by dividing the area of the current I(t) by the period of time (t). To determine the dc component of the output voltage, scale the average input current by R_{INT}.

$$Average\ Output\ Voltage\ (V_{OUTAVG}) = \alpha t_{OS}/t \times R_{INT} \quad (1)$$

Equation 1 becomes a linear function of the frequency when f_{IN} is substituted for 1/t.

$$V_{OUTAVG} = t_{OS} \times R_{INT} \times \alpha \times f_{IN} \quad (2)$$

Note that the relationship between the average output voltage and input frequency is a function of the one shot time constant and the integration resistor but the relationship is not a function of the integration capacitor because the integration capacitor is an open circuit to the dc. As shown in Equation 2, the most practical way to trim the full-scale voltage is to include a trim potentiometer in series with R_{INT}. Typically, a 30% trim range is required to absorb errors associated with t_{OS} and α.

It is also important to characterize the transient response of the integrator to determine the settling time of the FVC to a step change of input frequency. The transfer function of the lossy integrator is given in the frequency domain in the following equation:

$$\frac{V_{OUT}(S)}{I_{IN}(S)} = \frac{\frac{1}{C_{INT}}}{S + \frac{1}{R_{INT} \times C_{INT}}} \quad (3)$$

Where *S* is a complex number.

Equation 3 indicates that the natural or step response to a change of input frequency is governed by an exponential function with time constant $\pi = R_{INT} \times C_{INT}$.

When the average output voltage and transient response are known, use Equation 4 to determine the peak-to-peak output ripple. After determining the peak-to-peak output ripple, a design algorithm can be developed (see the References section).

Use the following equation to calculate the peak-to-peak output ripple:

$$V\ p-p = \frac{e^{(t_{OS}/R_{INT} \times C_{INT})} - e^{(t_{IN}/R_{INT} \times C_{INT})} + e^{(t_{IN}-t_{OS})/R_{INT} \times C_{INT}} - 1}{1 - e^{(t_{IN}/R_{INT} \times C_{INT})}} \times \alpha \times R_{INT} \quad (4)$$

where:
t_{OS} is the one shot time constant (sec).
R_{INT} is the integration resistor (Ω).
C_{INT} is the integration capacitor (*F*).
t_{IN} is the input time period ($1/f_{IN}$) (Hz).
α is the current amplitude (1 mA for AD650) (amps).

Equation 4 represents the peak-to-peak output ripple for a given design. The Design Procedure section discusses how this equation is used as an iterative part of the total solution. Equation 4 can also be used to illustrate how the ripple amplitude changes as a function of input frequency. The ripple amplitude changes only moderately with input frequency and has its largest magnitude at the minimum input frequency.

DESIGN PROCEDURE

As shown in Figure 3, the one shot on time is some fraction of the total input period. During the on time, the circuit integrates the current signal α. Keeping the current source on during the majority of this period minimizes the output ripple. Keeping the current source on is achieved by choosing the one shot time constant so that this constant occupies almost the full period of the input signal when this period is at its minimum (or when the input frequency is at its maximum). To design safely and allow for component tolerance at input f_{MAX}, make t_{OS} approximately equal to 90% of the minimum period. Using this value for t_{OS}, the value of the one shot timing capacitor, C_{OS}, is determined by the following equation:

$$C_{OS} = \frac{t_{OS} - 3 \times 10^{-7} \text{ sec}}{6.8 \times 10^{3} \text{ sec}/ F} \quad (5)$$

where t_{OS} is in sec and C_{OS} is in *F*.

For maximum linearity performance, use a low dielectric absorption capacitor for C_{OS}.

After determining C_{OS}, determine the integration resistor by using the full-scale equation (Equation 2) because t_{OS}, α, f_{IN}, and V_{OUT} are known. Determining the integration resistor leaves the integration capacitor as the final unknown value.

Choose C_{INT} by first determining the response time of the device being measured. If, for example, the frequency signal being measured is derived from a mechanical device, such as an aircraft turbine shaft, the momentum of the shaft and the blades must be used to determine the response time. The time constant of the FVC is then set to match the time constant of the mechanical system. The time constant of the FVC may be set somewhat lower, depending on the desired total response time of the mechanical and electrical system. Remember to allow several time constants (N) for the FVC to approach its final value. For the first iteration of C_{INT}, use the following expression:

$$C_{INT} = (Mechanical\ Response\ Time)/(N \times R_{INT}) \quad (6)$$

where *N* is the number of time constants chosen to allow adequate settling. Use Table 1 to determine the number of time constants required for a given settling accuracy.

Table 1. Settling Accuracy vs. Number of Time Constants

No. of Time Constants (N)	No. of Bits	% Accuracy
4.16	6	1.6
4.85	7	0.8
5.55	8	0.4
6.23	9	0.2
6.93	10	0.1
7.62	11	0.05
8.30	12	0.024
9.00	13	0.012
9.70	14	0.006
10.4	15	0.003
11.0	16	0.0015

A larger number of time constants gives a more responsive circuit, but the larger number also increases the ripple at the FVC output. A practical approach is to start with an 8-bit settling accuracy, use N = 6 time constants, and increase or decrease N depending on ripple content.

Use Equation 4 to calculate the ripple content. Remember that the ripple amplitude changes with frequency and is largest at the lowest frequency.

It is important to note that while in some cases the ripple amplitude may be large, the average value of the output voltage always represents the input frequency, unless the ripple gets too close and clips at the positive supply rail. Figure 4 shows an example of how output ripple amplitude changes with input frequency for a typical application. Figure 4 was obtained by plotting Equation 4 over the full range of input frequencies. For design purposes, it is only necessary to calculate ripple at the worst case frequency (f_{MIN}). The flowchart in Figure 5 summarizes the design procedure.

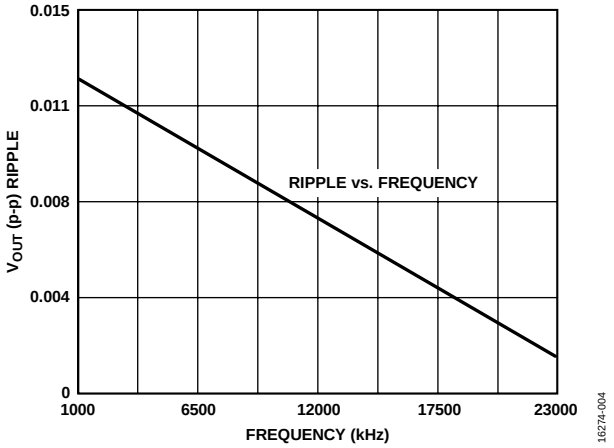

Figure 4. V_{OUT} (p-p) Ripple vs. Frequency (See the Design Example Section)

DESIGN EXAMPLE

The rpm of an automobile engine is monitored for use by an on-board computer. The rpm signal generated from an FVC is digitized with an 8-bit analog-to-digital converter (ADC). The rpm range of the engine extends from 300 rpm to 7000 rpm. A 200 tooth flywheel at these rotational speeds generates pulses from 1 kHz to 23 kHz. The response time to a step change in the throttle position of the engine is measured, in neutral, to be 400 ms. The goal is to design an FVC using the following steps that respond at approximately the same rate as (or faster than) the engine and has a ripple that is undetectable by the ADC. The ADC has a 10 V full-scale.

Let t_{OS} be $0.9 \times 1/f_{MAX} = 0.9 \times 43.5\ \mu s = 39\ \mu s$.

To determine the R_{INT} value, do the following:

1. Find that $C_{OS} = 0.0057\ \mu F$ using Equation 5. This value is an impractical value for polystyrene, but tantalum can be used with reduced linearity.
2. Using Equation 2, find that

$$R_{INT} = \frac{10\ V}{1\ mA \times 39\ \mu s \times 23\ kHz} = 11.14\ k\Omega \quad (7)$$

If R_{INT}, the load seen by the amplifier, is less than 1 kΩ, t_{OS} must be reevaluated. The following steps show how to adjust the C_{INT} value:

1. From Table 1, a resistor and capacitor (RC) network can settle to 8 bits in six time constants. Therefore,

$$C_{INT} = \frac{400\ ms}{(6)\,11.14\ k\Omega} = 6\ \mu F \quad (8)$$

2. Ripple = 6.25 mV at 300 rpm and 0.67 mV at 7000 rpm (from Equation 4).
3. Half of the LSB size for an 8-bit converter with 10 V full-scale is 19.5 mV. Fortunately, the ripple is below the quantization level on the first iteration. If desired, the integration capacitor may be lowered to reduce the response time of the FVC.
4. Guessing that $C_{INT} = 3.0\ \mu F$ or using an iterative computer program gives a maximum ripple content of 12.5 mV and a response time of 200 ms.

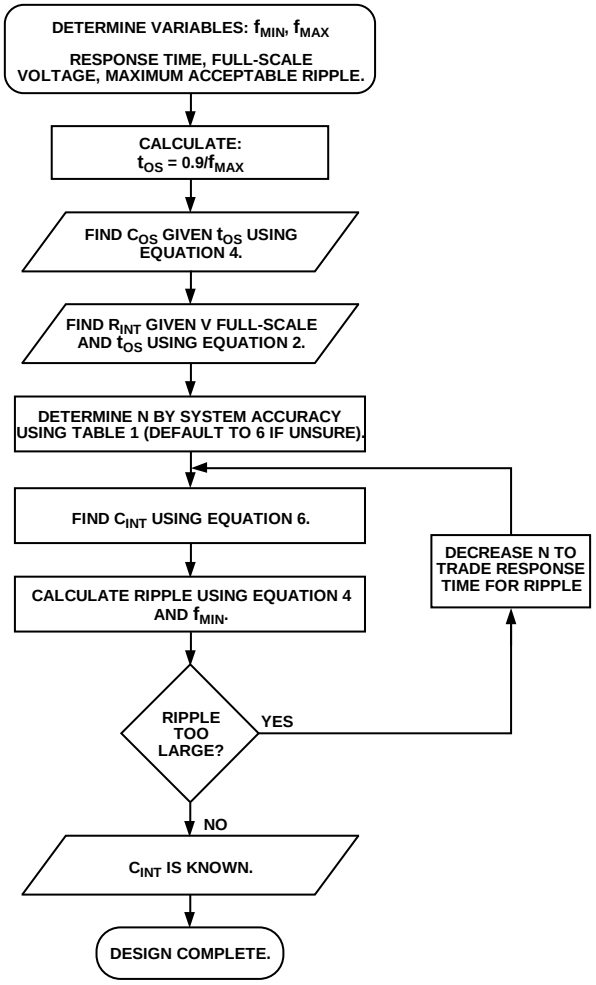

Figure 5. Design Flowchart

TRADE OFF BETWEEN RIPPLE AND RESPONSE TIME

In many cases, some compromises must be made between ripple and response time. If the response time is of primary importance, the integration capacitor may be lowered at the expense of increased ripple. Similarly, if ripple is of primary importance, the integration capacitor must be increased, resulting in slower response. The design procedure outlined in Figure 5 assumes that the ripple content is the less desirable effect. Rather than increasing C_{INT}, a low-pass filter can be used. However, using this filter slows the response time. An approximation to determine the total response time of two cascaded systems, each with separate response times, can be found by using the root sum of squares technique in the following equation:

$$t_{TOTAL} = \sqrt{t_A^{\,2} + t_B^{\,2}} \quad (9)$$

This technique leads to the three to one rule. That is, if t_A is more than three times t_B and the squares of t_A and t_B are added, t_B may be ignored. Therefore, t_A is the total response time of the system.

SUMMARY

Low cost VFCs can be used in FVC mode. Trade-offs exist between output settling time and ripple when the selection is application specific. However, by following the design guidelines outlined in this application note, it is possible to achieve optimized performance in many applications.

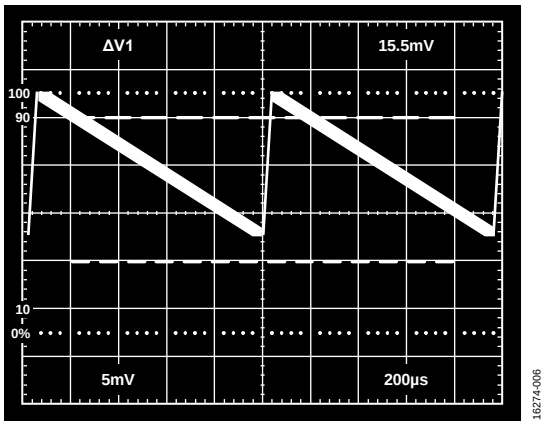

Figure 6. Typical Ripple Output

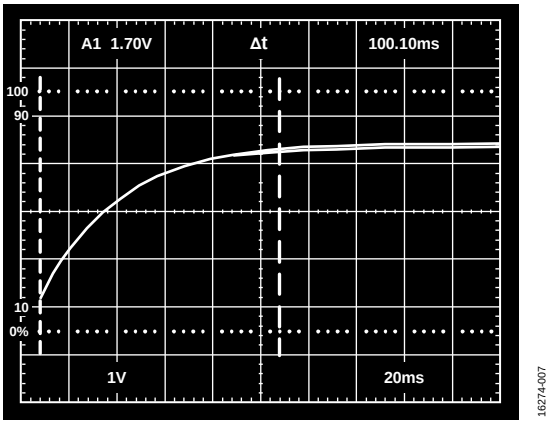

Figure 7. Response to Step Change in Frequency

REFERENCES

McGillem, C. D., and G. R. Cooper. 1984. *Continuous and Discrete Signal and System Analysis*, Second Edition. CBS College Publishing.