Instrumentation Applications for a Monolithic Oscillator

A Clock for All Reasons

Jim Williams

INTRODUCTION

Oscillators are fundamental circuit building blocks. A substantial percentage of electronic apparatus utilize oscillators, either as timekeeping references, clock sources, for excitation or other tasks. The most obvious oscillator application is a clock source in digital systems.[1] A second area is instrumentation. Transducer circuitry, carrier based amplifiers, sine wave formation, filters, interval generators and data converters all utilize different forms of oscillators. Although various techniques are common, a simply applied, broadly tunable oscillator with good accuracy has not been available.

Clock Types

Commonly employed oscillators are resonant element based or RC types.[2] Figure 1 shows two of each. Quartz crystals and ceramic resonators offer high initial accuracy and low drift (particularly quartz) but are essentially untunable over any significant range. Typical RC types have lower initial accuracy and increased drift but are easily tuned over broad ranges. A problem with conventional RC oscillators is that considerable design effort is required to achieve good specifications. A new device, the LTC1799, is also an RC type but fills the need for a simply applied, broadly tunable, accurate oscillator. Its accuracy and drift specifications fit between resonator based types and typical RC oscillators. Additionally, its board footprint, a 5-pin SOT-23 package and a single resistor, is notably small. Note that no external timing capacitor is required.

CLOCK TYPE	TYPICAL FREQUENCY ACCURACY	TYPICAL FREQUENCY RANGE	TUNABILITY	TEMPERATURE COEFFICIENT	POWER SUPPLY REJECTION RATIO	COMMENTS
Quartz	0.005%	10kHz to 200MHz	Poor	0.5ppm/°C Easily Achieved. See Comments	1ppm/V	High Stability and Initial Accuracy at Expense of Tunability. Essentially No Tunability. $1 \cdot 10^{-9}$ Stability Achievable with Compensation Techniques
Ceramic Resonator	0.5%	250kHz to 60MHz	Poor	30ppm/°C	20ppm/V	Lower Performance and cost than Quartz. Essentially Untunable
LTC1799	1.5%	1kHz to 33MHz	Good	40ppm/°C Plus Resistor Temperature Coefficient	500ppm/V	Add 10 to 50ppm/°C Temperature Coefficient, Depending on Resistor Type. Extremely Small Footprint— SOT-23 and 1 Resistor
Typical RC Based Clock	10%	1Hz to 25MHz	Good	200ppm/°C	2500ppm/V	Requires Careful Design and Component Selection for Best Results

Figure 1. LTC1799 Compared to Other Oscillators. Quartz and Ceramic Based Types Offer Higher Frequency Accuracy and Lower Drift but Lack Tunability. RC Designs are Tunable but Accuracy, Temperature Coefficient and PSRR are Poor

Note 1: Strictly speaking, an oscillator (from the Latin verb, "*oscillo*," to swing) produces sinusoids; a clock has rectangular or square wave output. The terms have come to be used interchangably and this publication bends to that convention.

Note 2: This forum excludes such exotica as rubidium and cesium based atomic resonance devices, nor does it admit mundane but dated approaches such as tuning forks.

A (Very) Simple, High Performance Oscillator

Figure 2 shows how simple to use the LTC1799 is. A single resistor (R_{SET}) programs the device's internal clock and pin-settable decade dividers scale output frequency. Various combinations of resistor value and divider choice permit outputs from 1kHz to 33MHz.[3] Figure 3 shows R_{SET} vs output frequency for the three divider pin states and the governing equation. The inverse relationship between resistance and frequency means that LTC1799 *period* vs resistance is linear.

Figure 4 reveals that the LTC1799 has speciated into a family. At present, there are two additional devices. The LTC6900, quite similar, cuts supply current to 500µA but gives up some frequency range. The LTC6902, designed for noise smoothed, multiphase power applications, has multiphase outputs and spread spectrum capability. Spread spectrum clocking distributes power switching over a settable frequency range, preventing significant noise peaking at any given point. This greatly reduces EMI concerns.

The LTC1799's combination of simplicity, broad tunability and good accuracy invites use in instrumentation circuitry. The following text utilizes the device's attributes in a variety of such applications.

Platinum RTD Digitizer

A platinum RTD, used for R_{SET} in Figure 5, results in a highly predictable O1 output period vs temperature. O1's output, scaled via counters, is presented to a clocked, period determining logic network which delivers digital output data. Over a 0°C to 100°C sensed temperature, 1000 counts are delivered, with accuracy inside 1°C. Extended range (sensor limits are –50°C to 400°C) is possible by using a monitoring processor to implement linearity correction in accordance with sensor characteristics.[4]

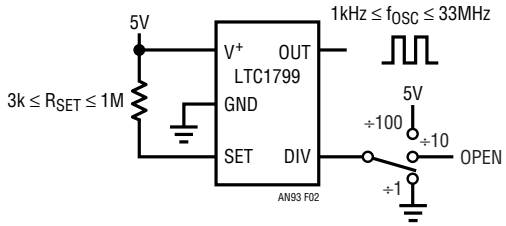


Figure 2. LTC1799 Oscillator Frequency Is Determined by R_{SET} and Divider Pin (DIV). Tunable Range Spans 1kHz to 33MHz

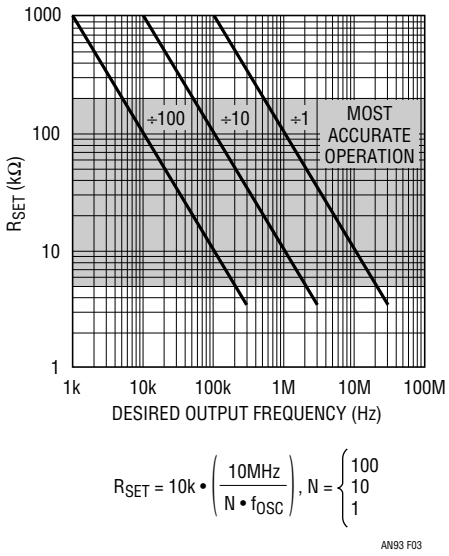


Figure 3. R_{SET} vs Output Frequency for the Three Divider Pin States and Governing Equation. Relationship between R_{SET} and Frequency Is Inverse; R_{SET} vs Period has Linear Characteristic

DEVICE TYPE	FREQUENCY RANGE	FREQUENCY ACCURACY	TEMPERATURE COEFFICIENT	PSRR	COMMENTS
LTC1799	1kHz to 33MHz	1.5%	40ppm/°C + Resistor Drift	0.05%/V	I_{SUPPLY} = 1mA
LTC6900	1kHz to 20MHz	1.5%	40ppm/°C + Resistor Drift	0.04%/V	Low Power (I_{SUPPLY} = 500µA) Version of LTC1799
LTC6902	5kHz to 20MHz	1.5%	40ppm/°C + Resistor Drift	0.04%/V	2-, 3- or 4-Phase Outputs. Programmable Width Spread Spectrum Frequency Modulation. Intended for Multiphase Power Supply Applications

Figure 4. Oscillator Family Details. LTC6900 Is Low Power Version of LTC1799. LTC6902, Intended for Noise Sensitive, High Power Switching Regulator Applications, Has Multiphase, Spread Spectrum Outputs. All Types Have Excellent Tunability, Good Frequency Accuracy, Low Temperature Coefficient and High PSRR

Note 3: This deceptively simple operation derives from noteworthy internal cleverness. See Appendix A, "LTC1799 Internal Operation" for a description.

Note 4: Linearity deviation over –50°C to 400°C is several degrees. See Reference 1.

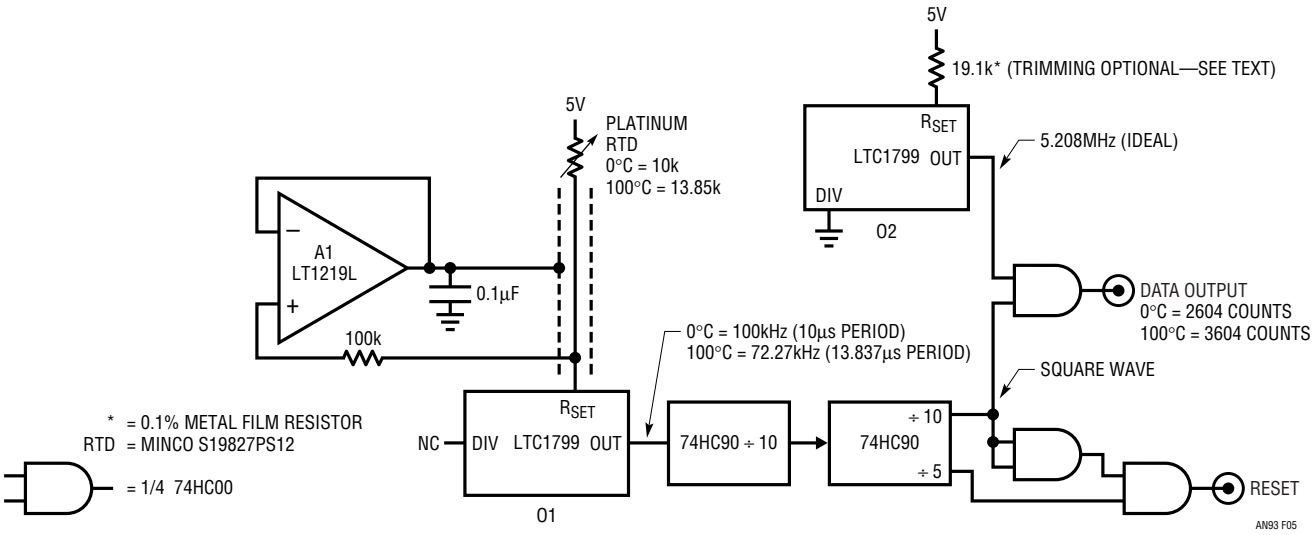


Figure 5. Platinum RTD Digitizer Accurate within 1° Over 0°C to 100°C. Platinum RTD Value Is Linearly Converted to Period by LTC1799. Logic and Second LTC1799 Clock Digitize Period into Output Data Bursts. A1 Drives RTD Shield at R_{SET} Potential, Bootstrapping Pin Capacitance to Permit Remotely Located Sensor

If the RTD is at the end of a cable, the cable shield should be driven by A1 as shown. This bootstraps the cable shield to the same potential as R_{SET}, eliminating jitter inducing capacitive loading effects at the R_{SET} node.[5]

Figure 6 shows operating waveforms. The RTD determines O1's output (Trace A), which is divided by 100 and assumes square wave form (Trace B). The logic network combines with O2's fixed frequency to digitize period measurement, which appears as output data bursts (Trace C). The logic also produces a reset output (Trace D), facilitating synchronization of monitoring logic.

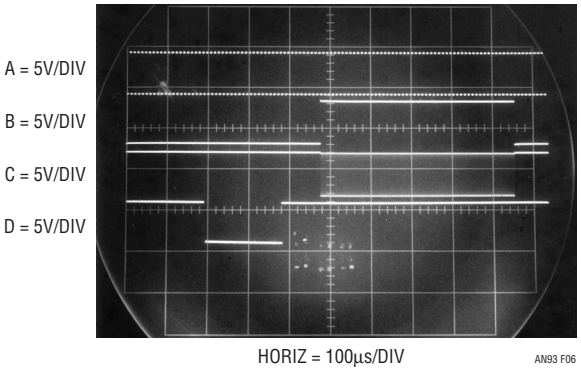


Figure 6. Platinum RTD Biased LTC1799 Produces Output (Trace A) which Is Divided by 100 (Trace B) and Gated with 5.2MHz Clock. Resultant Data Bursts (Trace C) Correspond to Temperature. Reset Pulse (Trace D), Preceding Each Data Burst, Permits Synchronization of Monitoring Logic

As shown, accuracy is about 1.5°C, primarily due to LTC1799 initial error. Obtaining accuracy inside 1°C involves simulating a 100°C temperature (13,850Ω) at the sensor terminals and trimming R_{SET} for appropriate output. A precision resistor decade box (e.g., ESI DB62) allows convenient calibration.

Thermistor-to-Frequency Converter

Figure 7's circuit also directly converts temperature to digital data. In this case, a thermistor sensor biases the R_{SET} pin. The LTC1799 frequency output is predictable, although nonlinear. The inverse R_{SET} vs frequency relationship combines with the thermistor's nonlinear characteristic to give Figure 8's data. The curve is nonlinear, although tightly controlled.

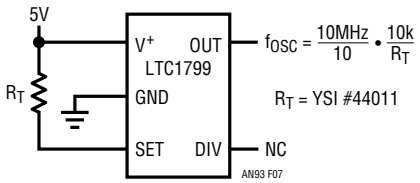


Figure 7. Simple Temperature-to-Frequency Converter Biases R_{SET} with Thermistor. Frequency Output Is Predictable, Although Nonlinear

Note 5: The R_{SET} node, while not unduly sensitive, requires management of stray capacitance. See Appendix B, "R_{SET} Node Considerations" for detail.

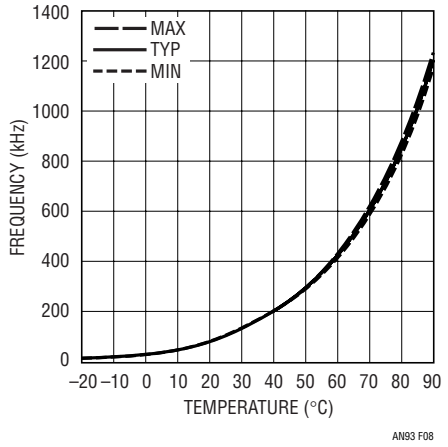
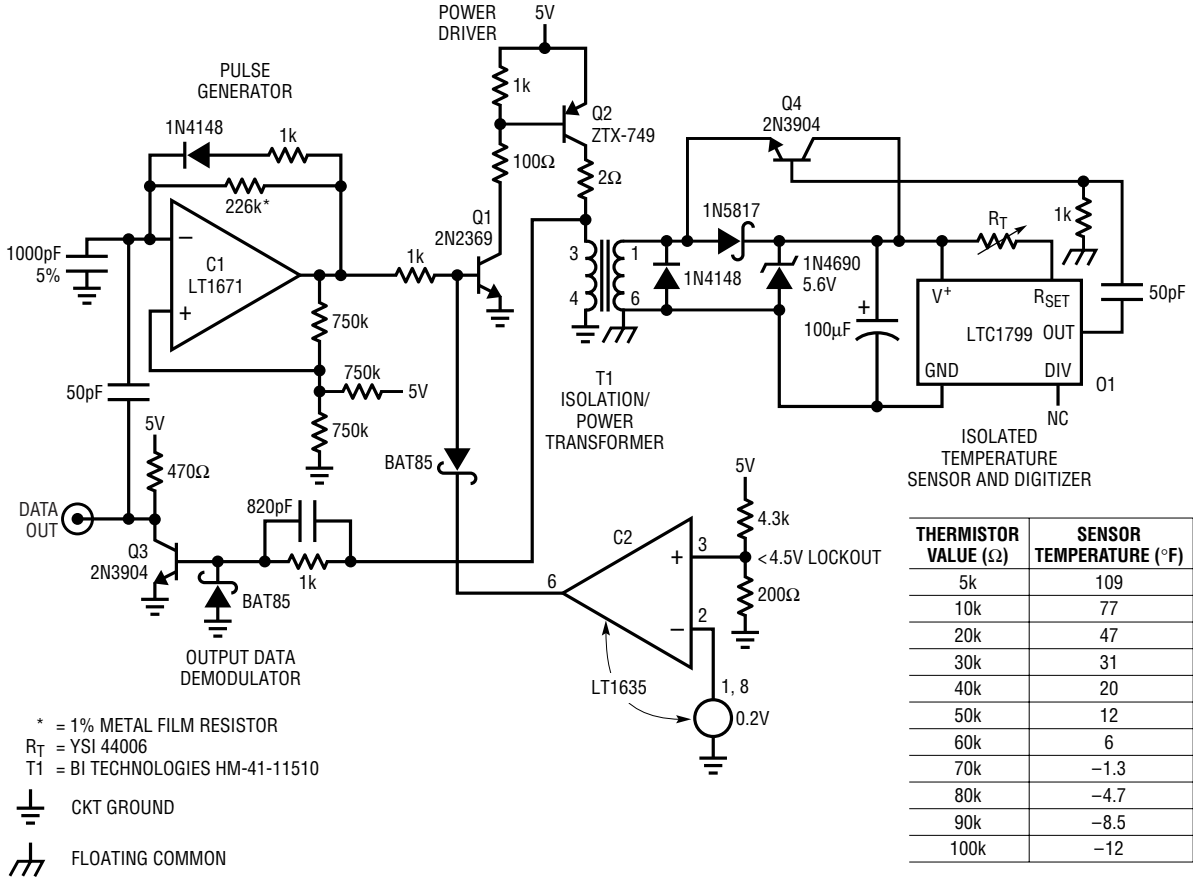


Figure 8. LTC1799 Inverse Resistance vs Frequency Relationship and Nonlinear Thermistor Characteristic Result in above Data. Curve Is Nonlinear, Although Tightly Controlled

Isolated, 3500V Breakdown, Thermistor-to-Frequency Converter

This circuit, building on the previous approach, galvanically isolates the thermistor from the circuit's power and data output ports. The 3500V breakdown barrier between the thermistor and power/data output ports permits operation at high common mode voltages. Such conditions are often encountered in industrial measurement situations.

Figure 9's pulse generator, C1, running around 10kHz, produces a 2.5µs wide output (Trace A, Figure 10). Q1-Q2 provide power gain, driving T1 (Trace B is Q2's collector). T1's secondary responds, charging the 100µF capacitor to a DC level via the 1N5817 rectifier. The capacitor powers O1, which oscillates at the sensor determined frequency. O1's output, differentiated to conserve power, switches Q4. Q4, in turn, drives T1's secondary, T1's primary receives Q4's signal and Q3 amplifies it, producing the circuit's data output (Trace C). Q3's collector also lightly



THERMISTOR VALUE (Ω)	SENSOR TEMPERATURE (°F)	OUTPUT FREQUENCY (Hz)
5k	109	2.01M
10k	77	1.01k
20k	47	505k
30k	31	337k
40k	20	253k
50k	12	203k
60k	6	168k
70k	–1.3	145k
80k	–4.7	127k
90k	–8.5	113k
100k	–12	101k

Figure 9. A Galvanically Isolated Thermistor Digitizer. C1 Sources Pulsed Power to Thermistor Biased LTC1799 via Q1, Q2 and T1. LTC1799 Output Modulates T1 through Q4. Q3 Extracts Data, Presents Ouput. T1's 3500V Breakdown Sets Isolation Limit

modulates C1's negative input (Trace D), synchronizing T1's primary drive to the data output. C2 prevents erratic circuit operation below 4.5V by removing Q1's drive.

C1's continuous clocking, while maintaining O1's isolated DC power supply, generates periodic cessations in the frequency coded output. These interruptions can be used as markers to control operation of monitoring logic. Output frequency vs thermistor characteristics are included in Figure 9.

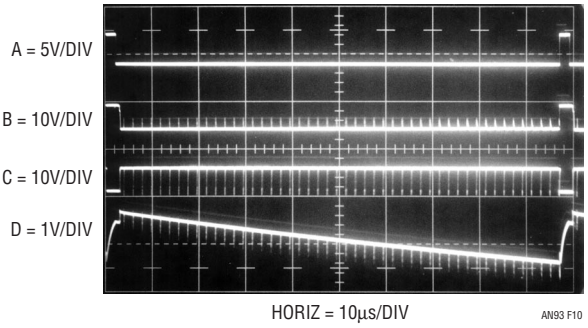


Figure 10. Isolated Thermistor Digitizer's Waveforms Include C1's Output (Trace A), Q2's Collector Drive to T1 (Trace B), Data Output (Trace C) and C1's Negative Input (Trace D). C1's Negative Input (Trace D) Is Lightly Modulated by Q3, Synchronizing Transformer Power Drive to Data Output

Relative Humidity Sensor Digitizer-Hetrodyne Based

Figure 11 converts the varying capacitance of a linearly responding relative humidity sensor to a frequency output. The 0Hz to 1kHz output corresponds to 0% to 100% sensed relative humidity (RH). Circuit accuracy is 2%, plus an additional tolerance dictated by the selected sensor grade. Circuit temperature coefficient is ≈400ppm/°C and power supply rejection ratio is <1% over 4.5V to 5.5V. Additionally, one sensor terminal is grounded, often beneficial for noise rejection.

This is basically a hetrodyne circuit. Two oscillators, one variable, one fixed, are mixed, producing sum and difference frequencies. The variable oscillator is controlled by the capacitive humidity sensor. The demodulated difference frequency is the output.[6] The hetrodyne frequency subtraction approach permits a sensed 0% RH to give a 0Hz output, even though sensor capacitance is not zero at RH = 0%.

C1, the sensor controlled variable oscillator, runs between the indicated output frequencies for the RH sensor excursion noted. The RH sensor is AC coupled, in accordance with its manufacturer's data sheet.[7] Reference oscillator O1 is tuned to C1's nominal 25% RH dictated frequency.

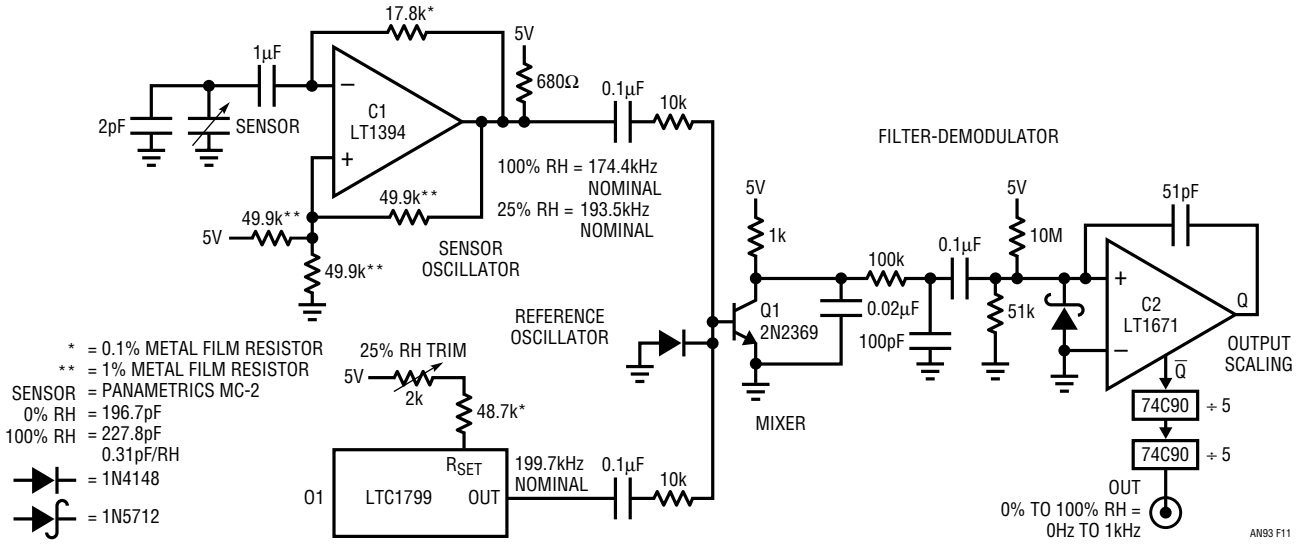


Figure 11. Hetrodyne Based Humidity Transducer Digitizer Has Grounded Sensor, 2% Accuracy. Capacitively Sensed Hygrometer Beats Humidity Dependent Oscillator (C1) Against Stable Oscillator O1. Difference Frequency Is Demodulated by Q1, Converted to Pulse Form at C2. Counters Scale Output for 0kHz to 1kHz = 0% to 100% Relative Humidity

Note 6: Hetrodyne techniques, usually associated with communications circuitry, have previously been applied to instrumentation. This circuit's operation was adapted from approaches described in References 2, 3 and 4.

Note 7: DC coupling introduces destructive electromigration effects. See Reference 6.

The two oscillators are mixed at Q1's base (Figure 12, Trace A). Q1 amplifies the mixed frequency components, although collector filtering attenuates the sum frequency. The RH determined difference frequency, appearing as a sine wave at Q1's collector (Trace B), remains. This waveform is filtered and AC coupled to zero crossing detector C2. AC hysteretic feedback at C2's input (Trace C) produces clean C2 output (Trace D). Counter based scaling at C2's output combines with slight sensor padding (note 2pF value across the sensor) to provide numeric output frequency correspondence to RH. Calibration involves simulating the RH sensor's 25% value and trimming O1 for a 250Hz output. The simulated value may be built up from known discrete capacitors or simply dialed out on a precision variable air capacitor (General Radio 1422D).

When evaluating circuit operation, it is useful to consider that C1's frequency changes inversely with sensor capacitance; its *period* is linear vs sensor capacitance. This would normally corrupt the desired linear output relationship between frequency and RH. Practically, because the sensor's excursion range is small compared to its 0% RH value, the error is similarly small. This term almost entirely accounts for the circuit's stated 2% accuracy.

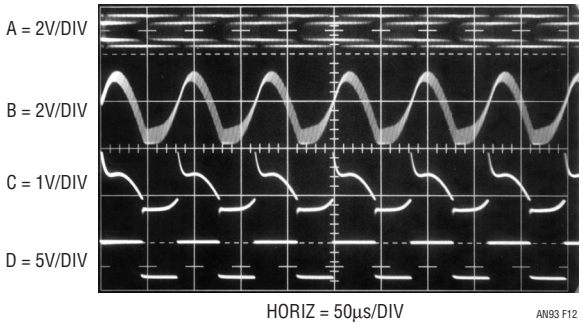


Figure 12. Sensor and Stable Oscillators are Mixed at Q1's Base (Trace A); Difference Frequency Appears at Q1's Collector (Trace B). Filtering and AC Hysteresis at C2's + Input (Trace C) Produce Clean Response at C2's Output (Trace D)

Relative Humidity Sensor Digitizer-Charge Pump Based

Figure 13 also digitizes the capacitive humidity sensor's output but has better specifications than the previous circuit. Circuit accuracy is 0.3%, plus the selected sensor grade's tolerance. Temperature coefficient is about 300ppm/°C and power supply rejection ratio is 0.25% for 5V ±0.5V. Compromises include a floating sensor and somewhat more complex circuitry.

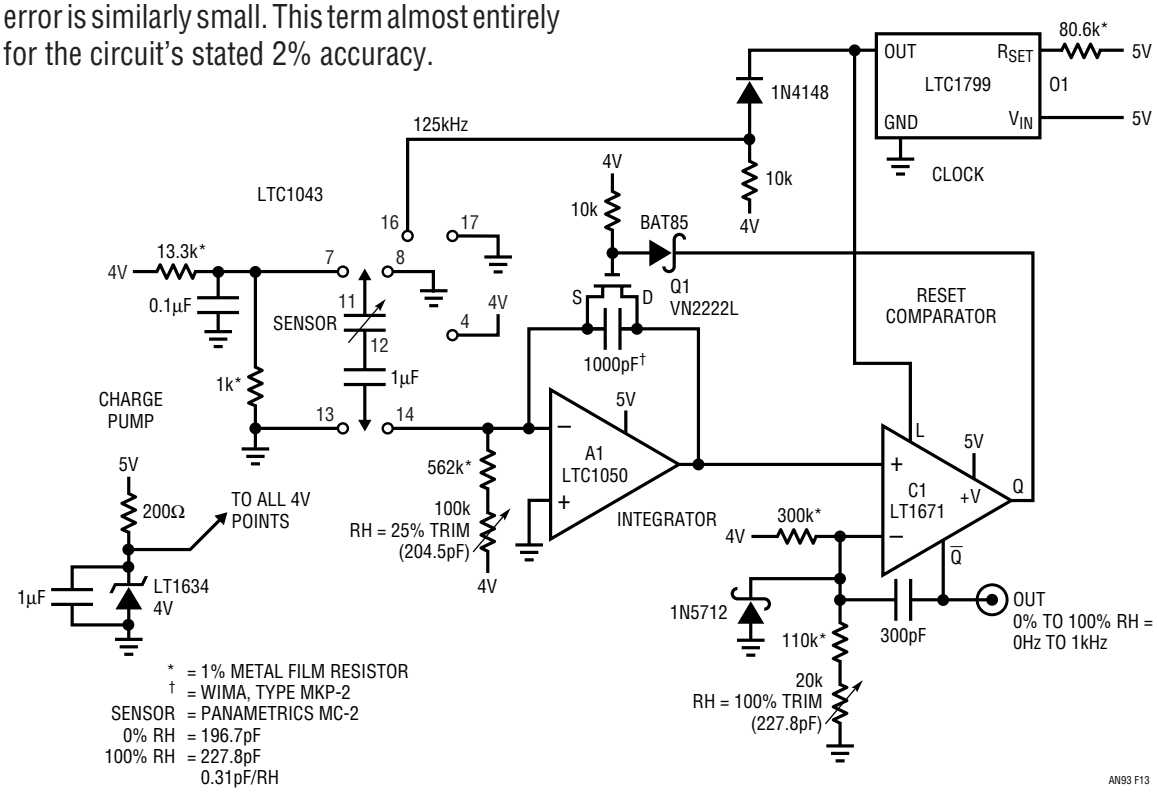


Figure 13. Hygrometer Digitizer Has 0.3% Accuracy, Although Sensor Must Float Off-Ground. Humidity Sensor Determines Charge Delivered to A1 Integrator During Each Charge Pump Cycle. Resultant A1 Output Ramp Is Reset by Level Triggered C1 via Q1. Output Frequency, Taken at C1, Varies with Humidity

O1 (Trace A, Figure 14) clocks an LTC1043 switch array based charge pump. This configuration alternately connects the AC coupled RH sensor to a 4V reference derived potential and then discharges it into A1's summing point. A1, an integrator, responds with a ramping output, Trace B of Figure 14. When A1's output exceeds C1's negative input voltage, C1's Q output (Trace C, Figure 14) goes high, triggering Q1 and resetting the ramp. AC feedback to C1's negative input (Trace D) ensures long enough Q1 on-time for complete ramp resent. This action's repetition rate depends on RH sensor value. The A1-C1 loop is synchronized to the charge pump's clocking by O1's output path to C1's latch input. In theory, if the charge pump, offset term (25% trim current) and ramp amplitude are tied to the same potential, this circuit does not require a voltage reference. In practice, the sensor's extremely small capacitance shifts magnify the effect of charge pump errors vs supply, necessitating powering the LTC1043 from the 4V reference. Once this is done, the mentioned points are tied to the 4V reference. Note that the 5V powered O1's output must be level shifted to drive the LTC1043.

A trimmed DC offset current (100k potentiometer) into A1's summing junction compensates the RH sensor's offset term (e.g., 0% RH ≠ 0pF). Output frequency is scaled by the 20kΩ trim at C1 so 0% to 100% RH = 0Hz to 1kHz. Trimming involves substituting capacitance for the sensor's known 100% and 25% values and trimming the appropriate adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. A precision variable capacitor (General Radio type 1422D) is invaluable in this regard, although acceptable results are possible with built-up calibrated discrete capacitors.

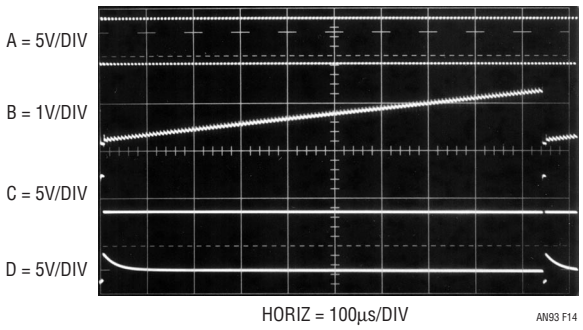


Figure 14. LTC1799 Clock (Trace A) Drives Humidity Sensor Based Charge Pump, Producing A1 Output Ramp (Trace B). C1 Q Output, Trace C, Biases Q1, Resetting Ramp. AC Feedback at C1 (Trace D) Permits Complete Ramp Reset, Sets Output Pulse Width

Relative Humidity Sensor Digitizer-Time Domain Bridge Based

Figure 15, also a relative humidity (RH) digitizer, features 1% accuracy, PSRR of 1% over 4.5V to 5.5V, temperature coefficient of 350ppm/°C and a ground referred sensor. Additionally, the circuit's trim scheme accommodates wide tolerance grade RH sensors. The circuit is basically a time domain bridge; it subtracts time intervals representing sensor and sensor offset values to determine sensor value extrapolated to RH = 0%. This measurement is digitized and scaled so zero to 100 counts equals 0% to 100% RH at the output.

O1's nominal 12.77MHz output, conditioned by a counter chain and an inverter configured gate, presents a 12.4kHz, 2.5µs pulse (Trace A, Figure 16) to Q1A and Q1B. The transistors' collectors fall (Trace B = Q1A collector – Trace C = Q1B collector) to zero volts. When the base drive ceases, both collectors ramp towards 5V. Trace B's ramp slope varies with the RH sensor's capacitance; Trace C's ramp slope represents the sensor's offset value (0% RH ≠ 0pF). C1 and C2 switch when their associated ramp inputs cross the comparators' common DC input potential. The comparator outputs (Trace D = C2, Trace E = C1) define a "both high" time region proportional to the ramp slopes' difference and, hence, an offset corrected version of sensor value. This time interval is gated with O1's output, providing Trace F's data output.

Circuit operation is fairly straightforward, although some details bear mention. Q1, a dual transistor, promotes cancellation of the individual transistors' V_{CE} vs temperature terms, minimizing their error contribution. The unit specified, a 2-die type, minimizes crosstalk; monolithic types should not be substituted. Similarly, a dual comparator should not be substituted for the single types specified for C1 and C2. Also, the comparators operate at high source impedance relative to their input characteristics but symmetry provides adequate error cancellation. Finally, the 5.6k resistor combines with the output gates' input capacitance, forming a ≈20ns lag. This delay prevents false output data transients when the ramps are resetting.

Trimming procedure is similar to the previous RH circuit. It involves substituting capacitance for the sensor's known 100% and 25% values and trimming the indicated adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. A precision variable capacitor (General Radio type 1422D) is invaluable for this work, although acceptable results are possible with calibrated discrete capacitor assemblies.

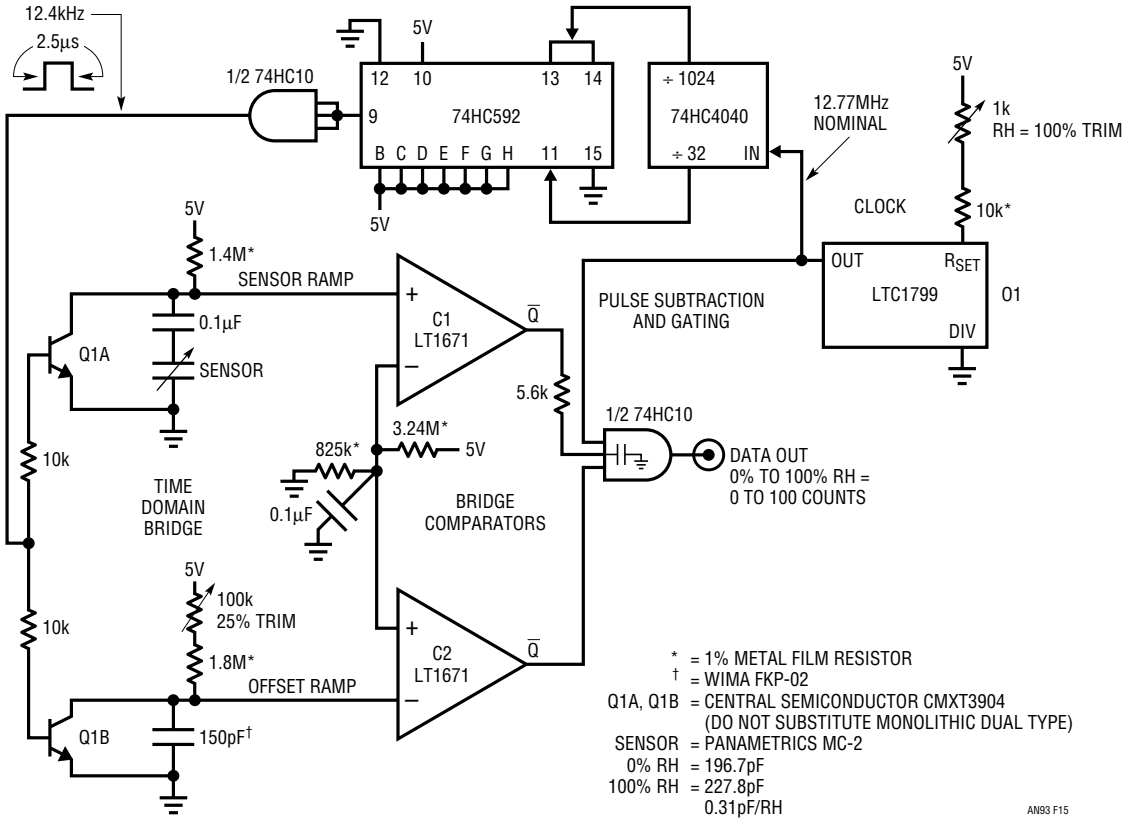


Figure 15. Humidity Transducer Digitizer Has Grounded Sensor, 1% Accuracy; Trim Scheme Allows Low Tolerance Sensors. Clocked Q1A-Q1B Configurations Produce Ramp Outputs. Q1A Ramp Slope Varies with Humidity Sensor Value, Q1B Ramp Represents Sensor's Offset (0% RH ≠ 0pF). C1, C2 Digitize Ramp Times. Gate Extracts Time Difference, Presents 0 to 100 Counts Out for 0% to 100% Relative Humidity

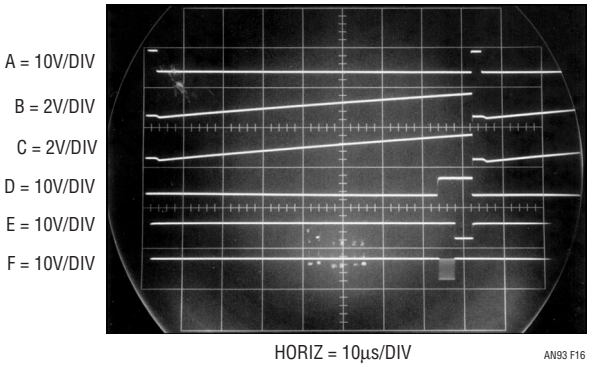


Figure 16. Humidity Sensor Time Domain Bridge Waveforms. Gate (Figure 15, Upper Left) Clocks (Trace A) Q1A and Q1B. Sensor and Offset Ramps Are Traces B and C. C1 and C2 Outputs are Traces D and E. Gate Extracts C1-C2 Time Difference, Presents Trace F's Digitized Output

40nV Noise, 0.05μV/°C Drift, Chopped Bipolar Amplifier

Figure 17's circuit, adapted from Reference 7, combines the low noise of an LT1028 with a chopper based carrier modulation scheme to achieve an extraordinarily low noise, low drift DC amplifier. DC drift and noise performance exceed any currently available monolithic amplifier. Offset is inside 1μV, with drift less than 0.05μV/°C. Noise in a 10Hz bandwidth is less than 40nV, far below monolithic chopper stabilized amplifiers. Bias current, set by the bipolar LT1028 input, is about 25nA. The circuit is powered by a single 5V supply, although its output will swing ±2.5V. Additionally, a carefully selected chopping frequency prevents deleterious interaction with 60Hz related components at the amplifier's input. These specifications suit demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

Ø1's 37kHz output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing A1 to see a chopped version of the input voltage. A1 amplifies this AC signal. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC coupled, its DC offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift noted. A1's input damper minimizes offset voltage contribution due to nonideal switch behavior.

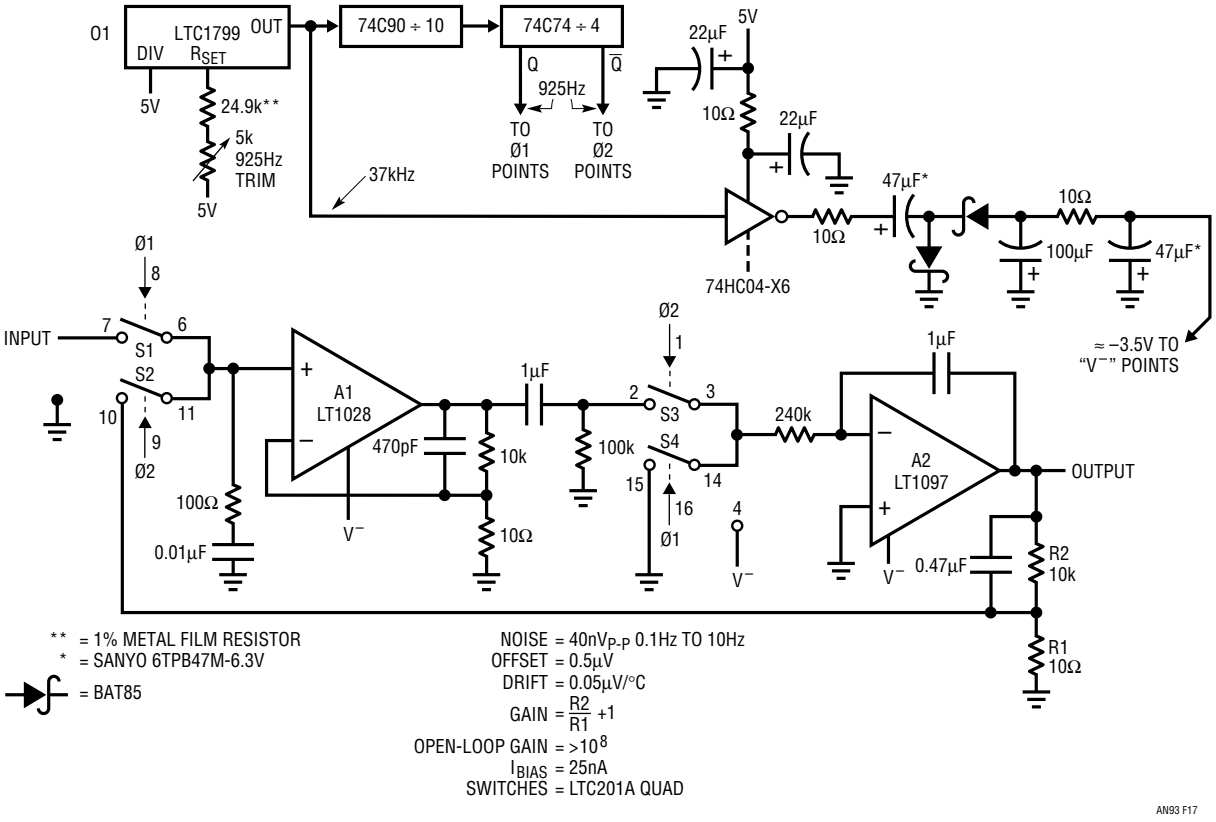


Figure 17. 5V Powered, Chopped Bipolar Amplifier. Noise Is ≈40nV with 0.05μV/°C Drift. DC Input Is Carrier Modulated, Amplified by A1, Demodulated to DC and Fed Back from A2. 925Hz Carrier Clock Prevents Interaction with 60Hz Line Originated Components. Negative Supply, Derived via Charge Pump, Allows Zero Volt Output Swing

Normally, this single supply amplifier's output would be unable to swing to ground. This restriction is eliminated by powering the circuit's negative rail from a charge pump. O1's 37kHz output excites the charge pump, comprised of paralleled logic inverters and discrete components. Deliberate 10Ω loss terms combine with the specified 47μF capacitors to form a very low noise power source. These precautions eliminate charge pump noise which might otherwise degrade amplifier noise performance.

Figure 18, a noise plot of the amplifier in a 0.1Hz to 10Hz bandwidth, shows about 40nV of peak-to-peak noise. A1 and the 60Ω resistance of S1-S2 contribute about equally to form this noise. When using this amplifier, it is important to realize that A1's bias current flowing through the input source impedance causes additional noise. In general, to maintain low noise performance, source resistance should be kept below 500Ω. Fortunately, transducers such as strain gauge bridges, RTDs and magnetic detectors are well below this figure.

45nV Noise, 0.05μV/°C Drift, Chopped FET Amplifier

Figure 19 replaces the previous circuit's input stage with a pair of extremely low noise J-FETs. In most other respects, circuit operation is similar. Noise increases very slightly, to ≈45nV, but bias current decreases to only 500pA—50 times lower than the previous circuit. The noise performance is especially noteworthy—it is almost 17 times better than currently available monolithic chopper stabilized amplifiers and nearly equals the best bipolar designs. Other performance specifications, appearing in the figure, are similar to Figure 17.

The 925Hz clock is retained, although this ±15V powered design uses zeners to derive internal ±5V points. The clock and logic run from 5V and the LTC201 switches use ±5V. The switches low voltage rails reduce charge injection, minimizing its effect on offset voltage. RC damper networks further attenuate parasitic switch behavior effects, resulting in the 1μV offset specification.

Noise measured over Figure 20's 50 second interval is about 45nV in a 0.1Hz to 10Hz bandwidth. This is spectacularly low noise for a J-FET based design and is directly attributable to the input pairs' die size and current density.[8]

Clock Tunable, Filter Based Sine Wave Generator

A feedback loop enclosed resonator can be made to oscillate. Figure 21's sine wave generator takes advantage of this and eliminates the need for an amplitude control loop. This circuit, a mildly modified form of the Regan resonant bandpass loop, is clock tunable and produces sine and cosine outputs.[9]

The LTC1060 switched capacitor filter is set up as a clock tunable bandpass filter with a Q of 10. O1 clocks the filter at 100kHz, resulting in a 1kHz bandpass. C1, switched by the sine output, supplies square wave drive to the filter input in regenerative fashion. The loop is self-sustaining, resulting in continuous sine wave outputs at the indicated points. Zener bridge clamping of C1's output stabilizes square wave amplitude applied to the filter and, hence, the sine wave outputs. This form of amplitude control eliminates AGC loop settling times and potential instabilities. Changes in O1's clock frequency permit bandpass tuning, with no amplitude shifts during or after tuning.

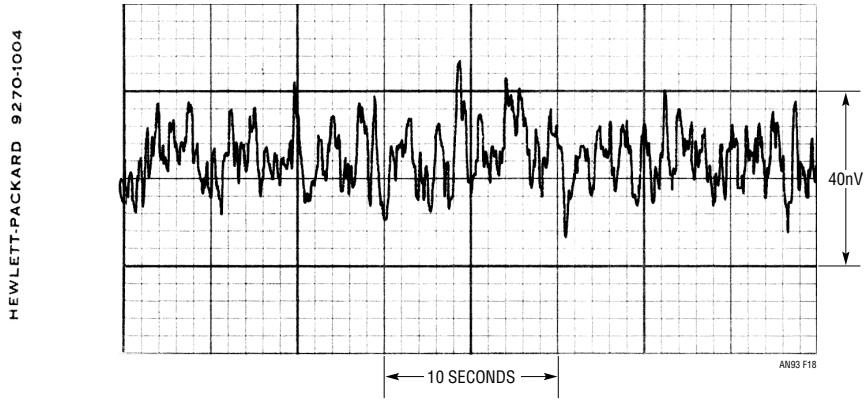


Figure 18. Noise in a 0.1Hz-10Hz Bandwidth Is about 40nV with 0.05μV/°C Drift

Note 8: See References 8 and 9.

Note 9: This circuit draws heavily on a scheme originated by Tim Regan. See Reference 10.

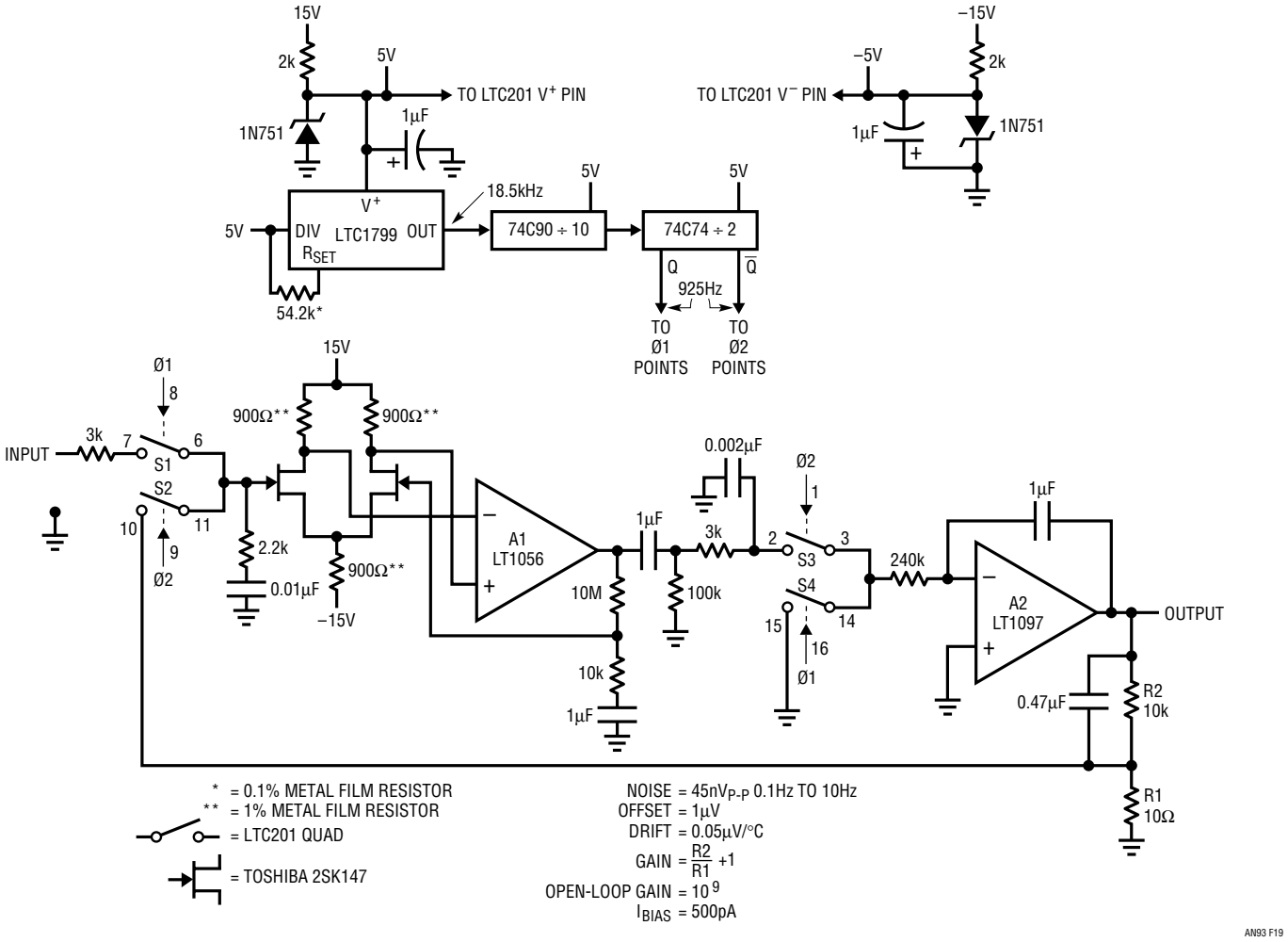


Figure 19. FET Input Version of Figure 17 Has 500pA Bias Current. 925Hz Clock Is Retained, Noise Increases Slightly to ≈45nV

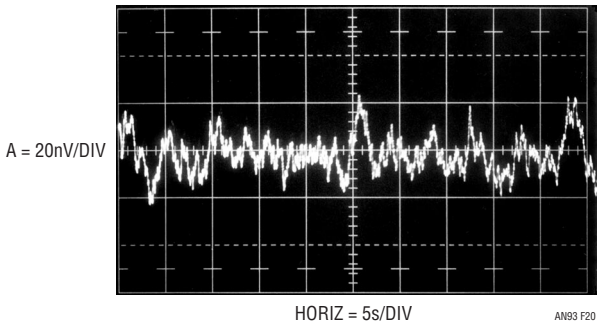


Figure 20. Chopped FET Input Amplifier Noise Is ≈45nV in 0.1Hz to 10Hz Bandwidth

Figure 22 shows operating waveforms. The bandpass filter, responding to C1's clamped output (Trace A), produces sine (Trace C) and cosine (Trace B) outputs. Distortion, Trace D, dominated by filter clock residue, is 2%.

Clock Tunable, Memory Based Sine Wave Generator

This circuit generates a variable frequency sine wave by continuously clocking a sine coded lookup table memory. The memory's state is converted to an analog output by a DAC. A strength of this technique is its rapid, high fidelity response to frequency and amplitude change commands.

O1, set to one of three output frequencies dictated by its digital control inputs, clocks the 74HC191 counters. These counters parallel load a 2716 EPROM programmed to produce an 8-bit (256 states) digitally coded sine wave. The program, developed by Sean Gold and Guy M. Hoover, appears in Figure 24.[10] The 2716's parallel output is fed to a DAC, producing the analog output.

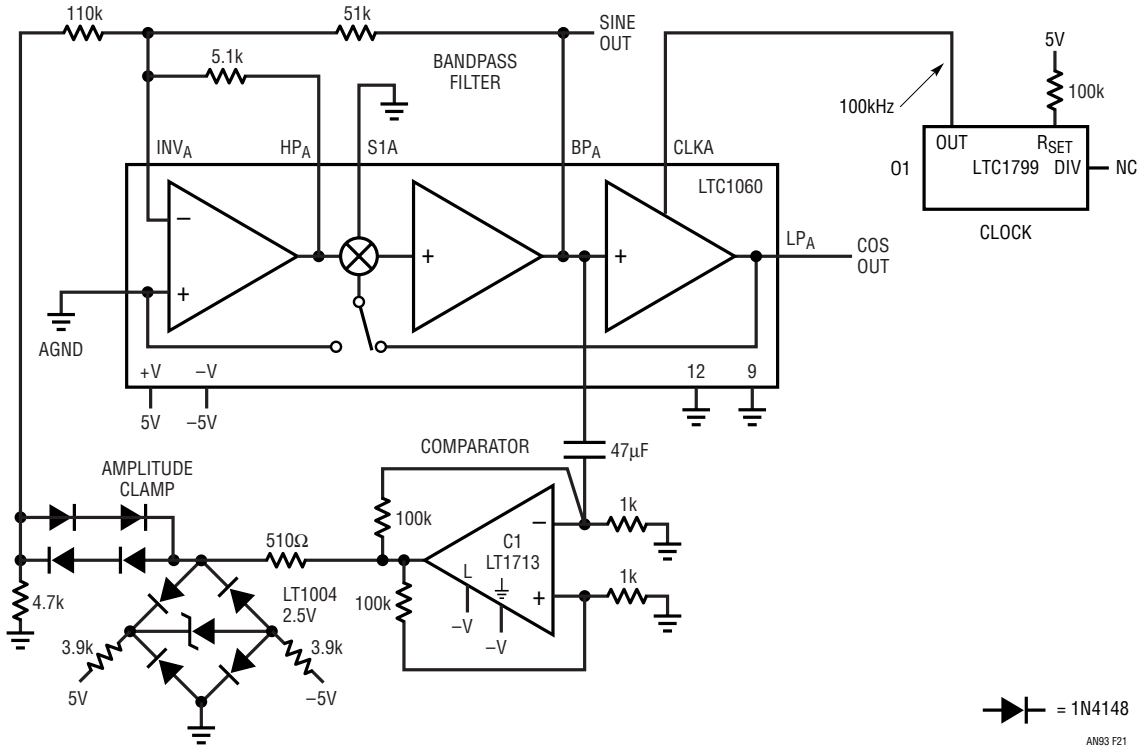


Figure 21. The Regan Resonant Bandpass Loop. A Bandpass Filter, Driven by C1's Oscillation Loop, Continuously Rings at Resonance. Clock Controls Output Frequency. Zener Bridge Clamp Sets Sine and Cosine Output Amplitude

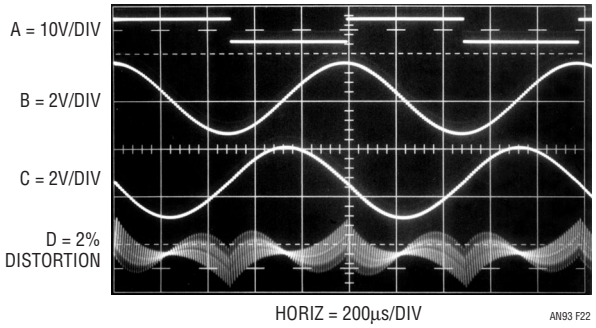


Figure 22. Bandpass Filter, Responding to C1's Loop Enforced Excitation (Zener Clamp Output, Trace A), Produces Sine (Trace C) and Cosine (Trace B) Outputs. Distortion (Trace D), Dominated by Switched Capacitor Filter Clock Residue, Is 2%

Note 10: See Reference 11.

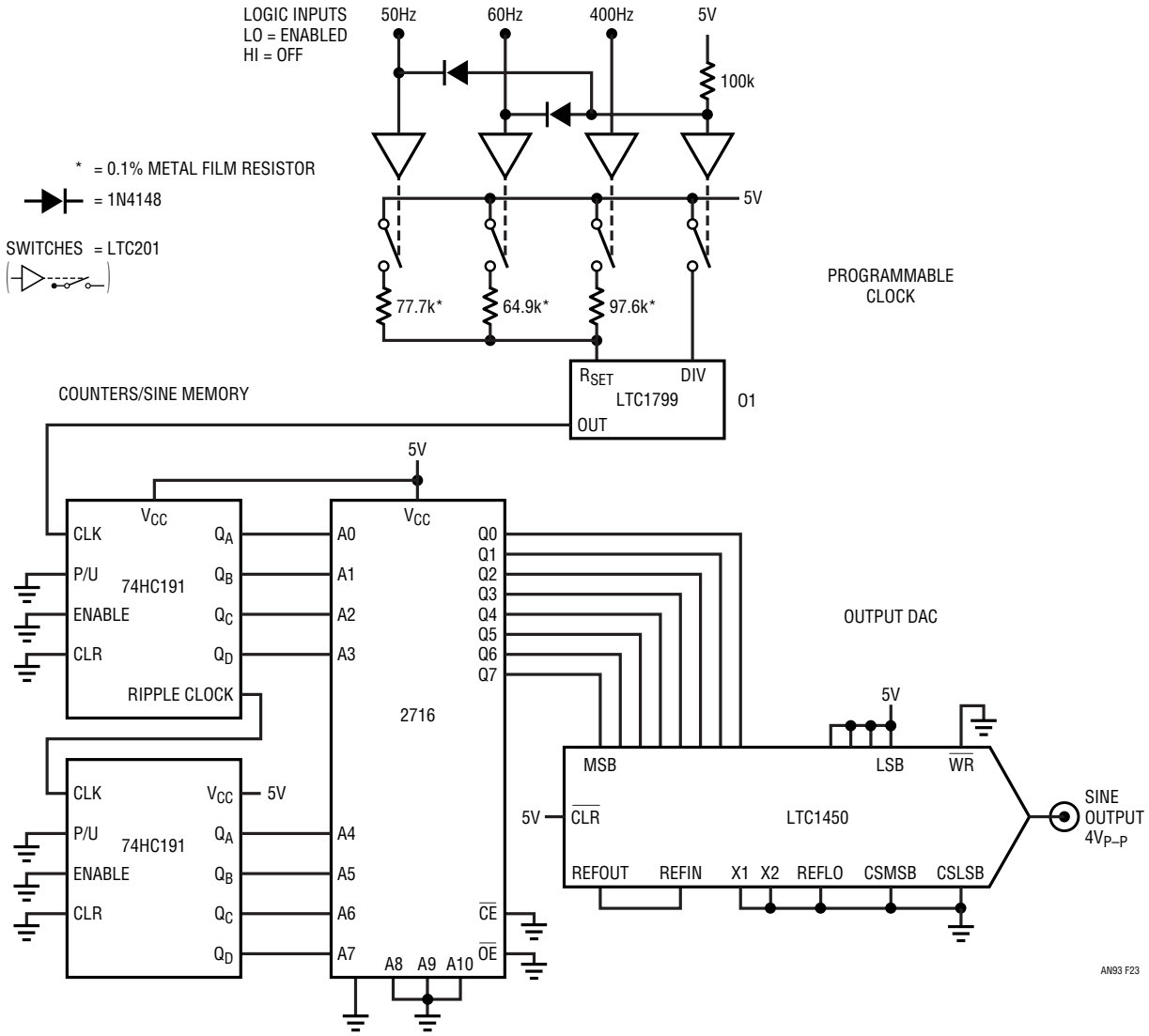


Figure 23. Counter Driven, Sine Encoded Memory Produces 0.75% Distortion Sinewave via D/A Converter. LTC1799 Oscillator Frequency, Controlled by Digital Inputs, Sets Output Frequency

```
Line 10736   Column   Wrap                  APL2/PC
      GENCODES
FF FF FF FF FE FE FE FD FD FC F8 FA F9 F9 F7 F6
F5 F4 F3 F1 F0 EE ED EB E9 E8 E6 E4 E2 E0 DE DC
D9 D7 D5 D2 D0 CE CB C9 C6 C3 C1 BE B9 B8 B6 B3
B0 AD AA A7 A4 A1 9E 9B 98 95 92 8E 8B 88 85 82
7F 7C 78 75 72 6F 6C 69 66 63 60 5D 5A 57 54 51
4E 4B 48 45 42 40 3D 3A 38 35 33 30 2E 2B 29 27
25 22 20 1E 1C 1A 18 17 15 13 11 10 0E 0D 0C 0A
09 08 07 06 05 04 03 03 02 02 01 01 00 00 00 00
00 00 00 00 01 01 02 02 03 03 04 05 06 07 08 09
0A 0C 0D 0E 10 11 13 15 17 18 1A 1C 1E 20 22 25
27 29 2B 2E 30 33 35 38 3A 3D 40 42 45 48 4B 4E
51 54 57 5A 5D 60 63 66 69 6C 6F 72 75 78 7C 7F
82 85 88 8B 8E 92 95 98 9B 9E A1 A4 A7 AA AD B0
B3 B6 B8 BB BE C1 C3 C6 C9 CB CE D0 D2 D5 D7 D9
DC DE E0 E2 E4 E6 E8 E9 EB ED EE F0 F1 F3 F4 F5
F6 F7 F9 F9 FA FB FC FD FD FE FE FE FF FF FF FF
```

Figure 24. Sinewave Generation Code for the Memory

Trace A in Figure 25 is the sine wave output, in this case tuned to 60Hz. Distortion, appearing as Trace B, is mostly composed of clock residue and measures about 0.75%. In Figure 26, the digital inputs abruptly change output frequency to 400Hz and then promptly return it to 60Hz. These frequency shifts occur crisply, with no alien components or untoward behavior. Amplitude shifts, accomplished by driving the DAC's reference input (see LTC1450 data sheet), are similarly well behaved. Figure 27 shows Trace B's amplitude faithfully responding to Trace A's DAC reference input step. As before, the lack of control loop time constants promotes uncorrupted response.

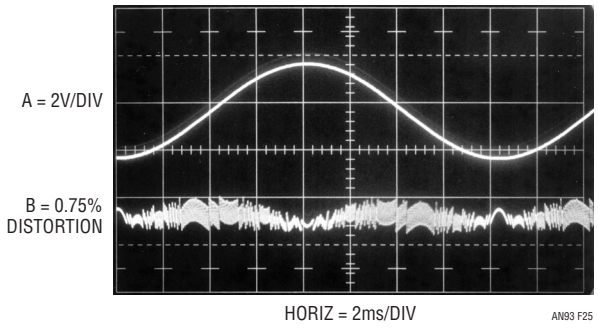


Figure 25. Sinewave Output (Trace A) and Its Distortion (Trace B). Clock Related Products Are Evident in Distortion Presentation

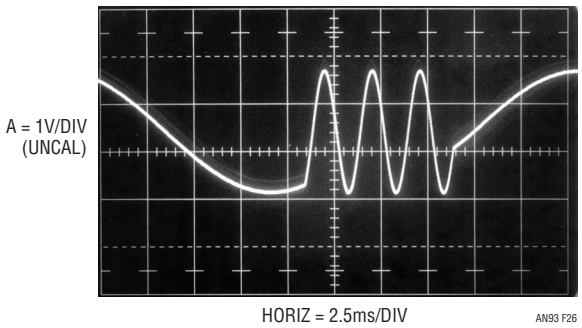


Figure 26. Fast Oscillator Frequency Shifting Permits Crisp Sinewave Output Frequency Change

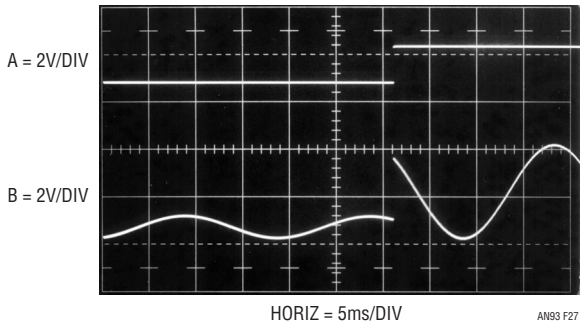


Figure 27. Trace B's Sinewave Amplitude Instantaneously and Faithfully Responds to DAC Reference Input Step, Trace A

Clock Tunable Notch Filter

Figure 28 shows a quick, clean way to tune a notch filter's center frequency by varying a single resistor, which could be switched. The LTC1062 switched capacitor filter and A1 form a clock tunable notch (see LTC1062 data sheet). O1, running from the 5V supply, furnishes the clock, which is level shifted by Q1 to drive the ±5V powered LTC1062. In this case, three common notch frequencies are listed; others are selectable by tuning O1 in accordance with the equivalency listed.

R	CLOCK FREQUENCY	NOTCH CENTER FREQUENCY
210k	4.75kHz	60Hz
249k	3.96kHz	50Hz
31.5k	31.72kHz	400Hz

$\frac{R1}{R2} = 1.234, \frac{f_{CLOCK}}{f_{NOTCH}} = \frac{79.3}{1}$

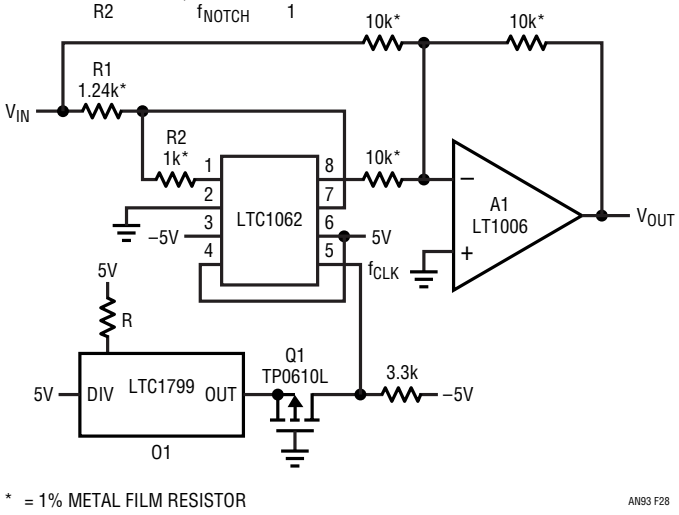


Figure 28. A Clock Tuned, Highly Selective Notch Filter. LTC1799 Oscillator Sets Notch Center Frequency According to Table. R Value Could be Switched Under Digital Control

Figure 29 shows notch performance at a 60Hz center frequency. Response is down over 45dB at 60Hz, with steep slopes on either side of the notch. This characteristic is maintained as center frequency is clock-tuned over broad ranges.

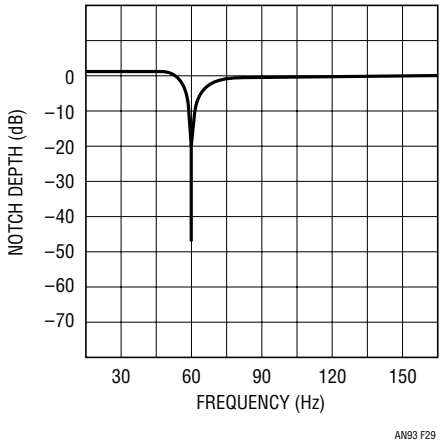


Figure 29. Notch Characteristic at 60Hz Center Frequency. Response Is Essentially Identical as Center Frequency Is Tuned over Broad Range

Clock Tunable Interval Generator with 20×10^6:1 Dynamic Range

An accurate interval generator with large dynamic range appears in Figure 30.[11] The circuit is made up of a clock, a counter and a dual flip-flop. Clock frequency and counter modulo are programmable. A trigger input is passed to flip-flop 1's $\overline{Q}$ output (Trace A, Figure 31) synchronously with O1's clock (Trace C). This output going low sets flip-flop 2's Q output, a circuit output, high (Trace B). Simultaneously, flip-flop 2's $\overline{Q}$ output resets the 4060 counter, allowing it to accumulate clock pulses (again, Trace C). When enough clock pulses occur to set the selected 4060 output high, flip-flop 2's clear input (Trace D) is pulled low, ending the circuit's output width. The output width is settable by O1's frequency and the counter's modulo, both variable over many decades. As shown, the interval is programmable over 800 nanoseconds to 16 seconds, although other counters can extend this range. Interval accuracy and stability is almost entirely dependent on O1's programming resistor.

8-Bit, 80µs, Passive Input, A/D Converter

In general, monolithic A/D converters have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, output data format, control protocol or economic constraints. Figure 32's 8-bit design has 90ppm/°C drift (<1LSB 0°C to 70°C) and converts in 80µs. The circuit consists of a current source, an integrating capacitor, a comparator, logic and a clock.[12]

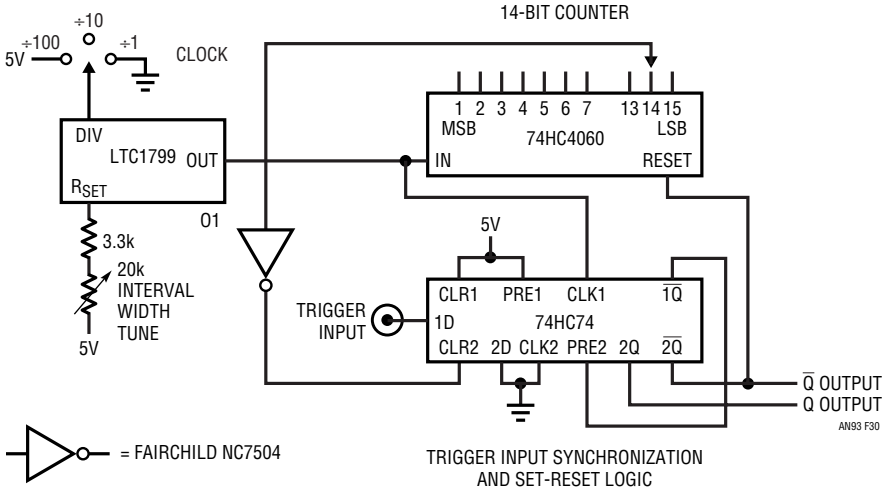


Figure 30. 1% Accurate Interval Generator with 20×10^6:1 Dynamic Range. Flip-Flop Output, Set by Trigger Input, Resets when Counter Times Out. LTC1799 Oscillator Controls Timing Sequence

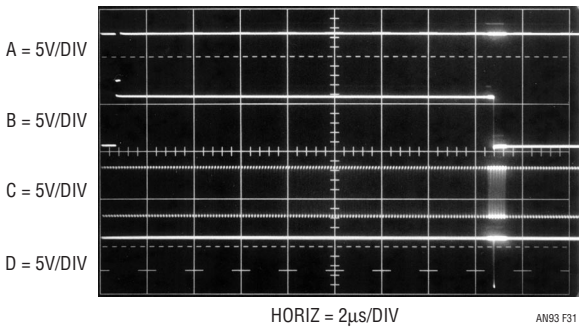


Figure 31. Trace A's Trigger Pulse Sets Circuit Output (Trace B) High. LTC1799 Oscillator (Trace C) Clocks Counter until Selected Counter Output Biases Inverter Low (Trace D), Resetting Circuit Output (Trace B). Reset Sequence Intensified for Photographic Clarity

Note 11: Pedestrian laboratory argot for interval generator is "one shot."

Note 12: This circuit is a modern incarnation of the earliest electronic A/D known to the author. See Reference 13.

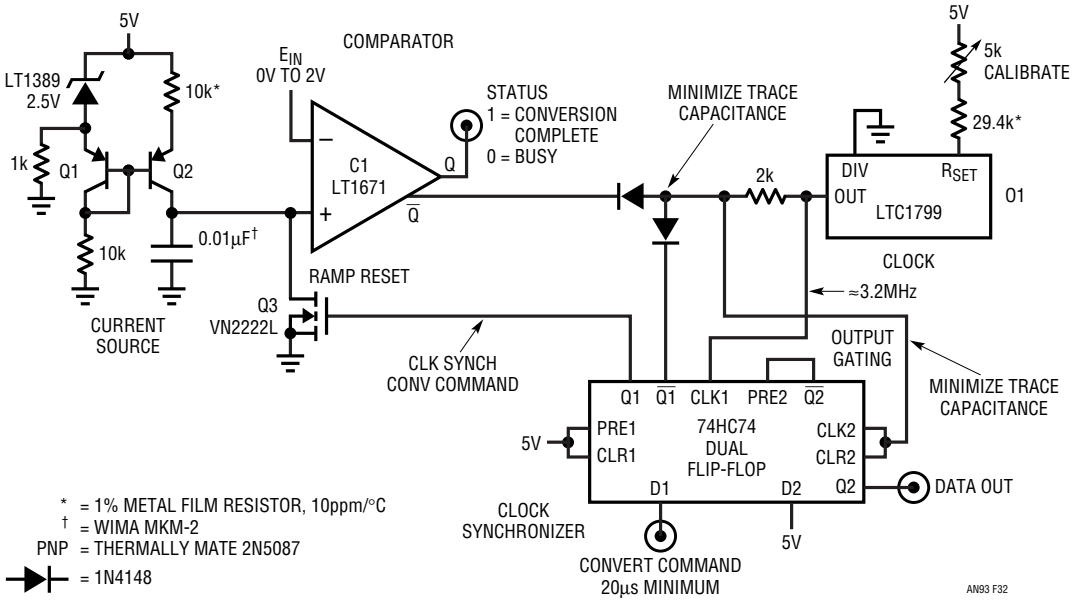


Figure 32. Simple 8-Bit A/D Converter Has Passive, High Impedance Input. Additional Features Include 80µs Conversion Time, Accurate 0°C to 70°C Operation

Applying a pulse to the convert command input causes flip-flop Q1 output to go high (Trace A, Figure 33) when the CLK1 input is clocked by O1. This turns on Q3, resetting the 0.01µF capacitor (Trace B). Simultaneously, $\overline{Q1}$ goes low, pulling the CLK2-CLR2 input down. C1's Q output, the circuit's status output (Trace C), also goes low and C1's $\overline{Q}$ output rises high. This logic state prevents any of O1's clock pulses from being transmitted to the circuit's data output (Trace D). When the convert command falls, Q1 goes low, Q3 turns off and the 0.01µF capacitor begins to ramp. Concurrently, $\overline{Q1}$ goes high, allowing clock pulses to appear at the data output. When the ramp crosses E_{IN}'s voltage, C1's outputs exchange state, pulling the CLK2-CLR2 line low and data output pulses cease. Thus, the O1 originated clock burst appearing at the data output is directly and solely proportional to E_{IN}. For the arrangement shown, 256 pulses appear for a 2V full-scale input. Conversion time decreases with the time required for the ramp to cross E_{IN}. A full-scale conversion requires 80µs, linearly descending to 8µs at 0.1 scale.

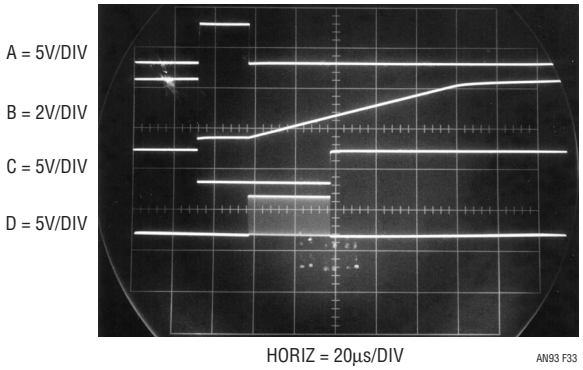


Figure 33. 8-Bit A/D Converter Waveforms (E_{IN} = 1V) Include Synchronized Convert Command (Trace A), Reference Ramp (Trace B), Status Output (Trace C) and Data Output (Trace D). Conversion, Initiable when Status Output Is High, Begins when Command Line Goes Low

Flip-flop 2, connected as a logic buffer, duplicates the high impedance diode-2kΩ node's logic state. As such, this node's trace capacitance should be minimized. This is facilitated by locating the diodes and 2k resistor adjacent to the CLK2-CLR2 inputs. Circuit trimming is accomplished by applying a 2V input and adjusting O1's frequency output ("calibrate") for 256 data output pulses per conversion.

Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

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APPENDIX A

LTC1799 INTERNAL OPERATION

As shown in Figure A1, the LTC1799's master oscillator is controlled by the ratio of the voltage between the V^+ and SET pins and the current entering the SET pin (I_{RES}). The voltage on the SET pin is forced to approximately 1.13V below V^+ by the PMOS transistor and its gate bias voltage. This voltage is accurate to ±7% at a particular input current and supply voltage (see Figure A2). The effective input resistance is approximately 2k.

A resistor R_{SET}, connected between the V^+ and SET pins, "locks together" the voltage ($V^+ - V_{SET}$) and current, I_{RES}, variation. This provides the LTC1799's high precision. The master oscillation frequency reduces to:

$$f_{MO} = 10MHz \bullet \left(\frac{10k\Omega}{R_{SET}}\right)$$

The LTC1799 is optimized for use with resistors between 10k and 200k, corresponding to master oscillator frequencies between 0.5MHz and 10MHz. Accurate frequencies up to 20MHz (R_{SET} = 5k) are attainable if the supply voltage is greater than 4V.

To extend the output frequency range, the master oscillator signal may be divided by 1, 10 or 100 before driving OUT (Pin 5). The divide-by value is determined by the state of the DIV input (Pin 4). Tie DIV to GND or drive it below 0.5V to select ÷1. This is the highest frequency range, with the master output frequency passed directly to OUT. The DIV pin may be floated or driven to midsupply to select ÷10, the intermediate frequency range. The lowest frequency range, ÷100, is selected by tying DIV to V^+ or driving it to within 0.4V of V^+. Figure A3 shows the

relationship between R_{SET}, divider setting and output frequency, including the overlapping frequency ranges near 100kHz and 1MHz.

The CMOS output driver has an on resistance that is typically less than 100Ω. In the ÷1 (high frequency) mode, the rise and fall times are typically 7ns with a 5V supply and 11ns with a 3V supply. These times maintain a clean square wave at 10MHz (20MHz at 5V supply). In the ÷10 and ÷100 modes, where the output frequency is much lower, slew rate control circuitry in the output driver increases the rise/fall times to typically 14ns for a 5V supply and 19ns for a 3V supply. The reduced slew rate lowers EMI (electromagnetic interference) and supply bounce.

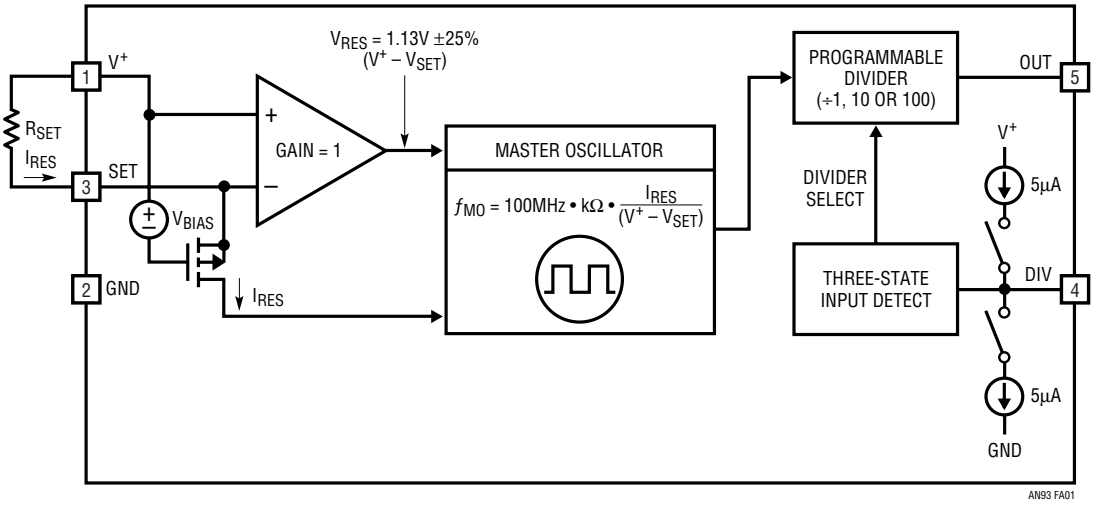


Figure A1. LTC1799 Master Oscillator Frequency Is Controlled by Ratio of Voltage Between V+ and SET and Current Entering SET. Pin-Programmable Frequency Divider Permits Output Frequency Ranging

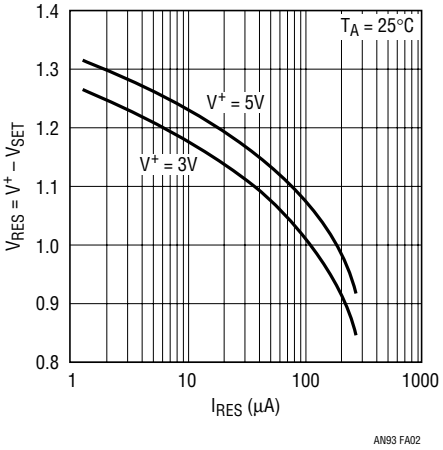


Figure A2. $V^+ - V_{SET}$ Variation with I_{RES}

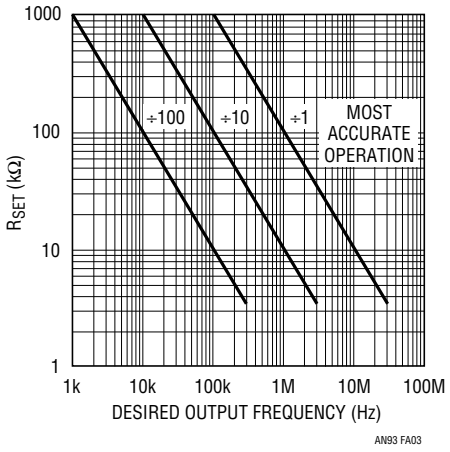


Figure A3. R_{SET} vs Desired Output Frequency for Three Output Divider Settings

APPENDIX B

R_{SET} NODE CONSIDERATIONS

The R_{SET} node is the LTC1799's sole analog input. Figure B1, a partial LTC1799 block diagram (see Appendix A for more detail) shows that the node is a MOSFET source and an amplifier input. Equivalent input resistance is about 2kΩ and the point sits approximately 1.13V below the LTC1799 V^+ pin. Excessive stray capacitance or noise at R_{SET} will influence amplifier operation, causing master oscillator jitter. Stray capacitance at R_{SET} should be limited to <10pF and signal lines, particularly those operating at high speed, should be routed away from R_{SET}. A simple guideline is to place the programming resistor directly at R_{SET}. In cases where R_{SET} is a transducer (e.g., a temperature sensor), it may be desirable to locate the transducer at the end of cable. Maintaining low effective capacitance at the R_{SET} node requires "bootstrap" driving the cable shield at the R_{SET} potential (Figure B2). This negates the effect of shield capacitance, because charge cannot transfer between it and R_{SET}. An amplifier capable of driving the shield is required but this is accomodatable. Text Figure 5 is a practical incarnation of this technique.

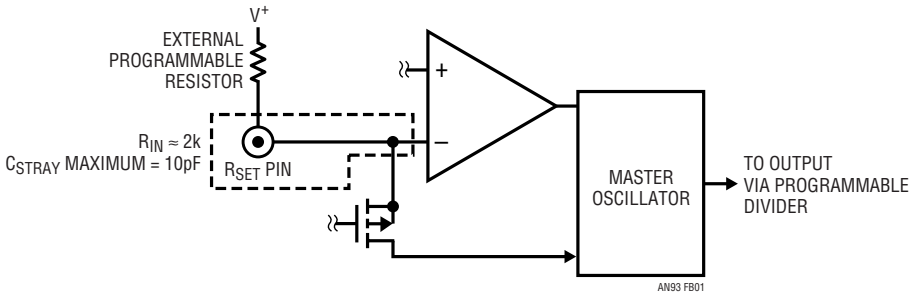


Figure B1. R_{SET} Pin Has Effective Input Resistance of ≈2k. Stray Pin Capacitance Must be <10pF to Avoid Output Frequency Jitter

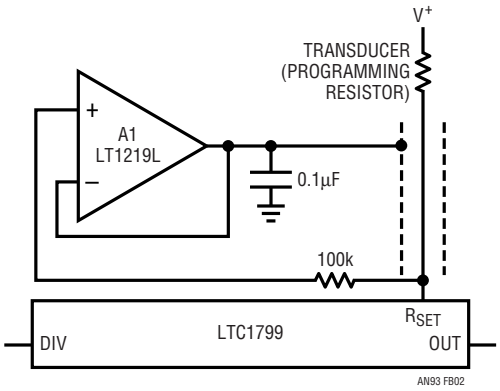
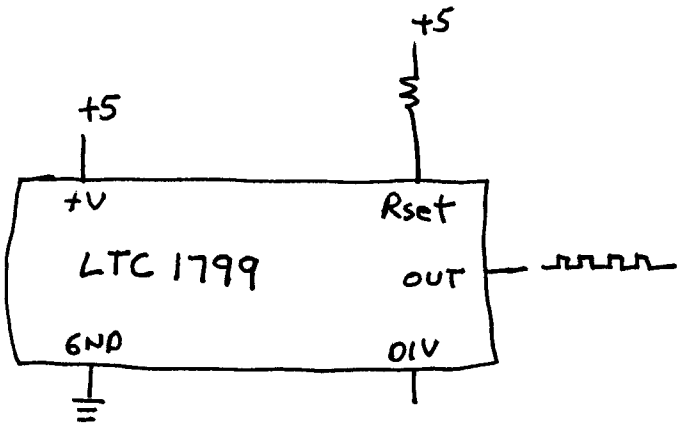


Figure B2. A1 Senses R_{SET} Voltage, Bootstraps Cable Drive Potential. Arrangement Prevents Cable Capacitance from Influencing R_{SET} Node Because Charge Cannot Transfer. 100k Resistor Isolates A1's Input and Trace Capacitance



"Everything should be as simple as possible, but not too simple."

— Einstein

'03

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