AN-634
APPLICATION NOTE

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Using the ADN2830 Evaluation Board

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INTRODUCTION

This application note describes the electrical evaluation board Rev. B kit for ADN2830 continuous wave (CW) laser driver. This application note shows how to configure the evaluation board to evaluate the ADN2830 electrically.

GENERAL DESCRIPTON

The ADN2830 is a CW laser driver, which provides closed-loop control of a laser at average optical power over time and over temperature after factory calibration. When used in conjunction with a laser, a monitor photo diode (MPD) current is required to control the average optical power emanating from the laser.

Because a laser emanates an optical average power when a bias current passes through the laser diode, an MPD then generates and sends a current to the ADN2830 for the optical average power control. In this evaluation board kit, a current mirror circuit replaces the expensive laser diode to evaluate the ADN2830 in an electrical configuration.

Each ADN2830 can provide up to 200 mA bias current. The evaluation board features an option to choose between sinking and sourcing the bias current. Three LEDs indicating power supply, degrade, and fail are available. The required power supply to the evaluation board is 5 V only.

DIGITAL PICTURE OF THE ADN2830 EVALUATION BOARD

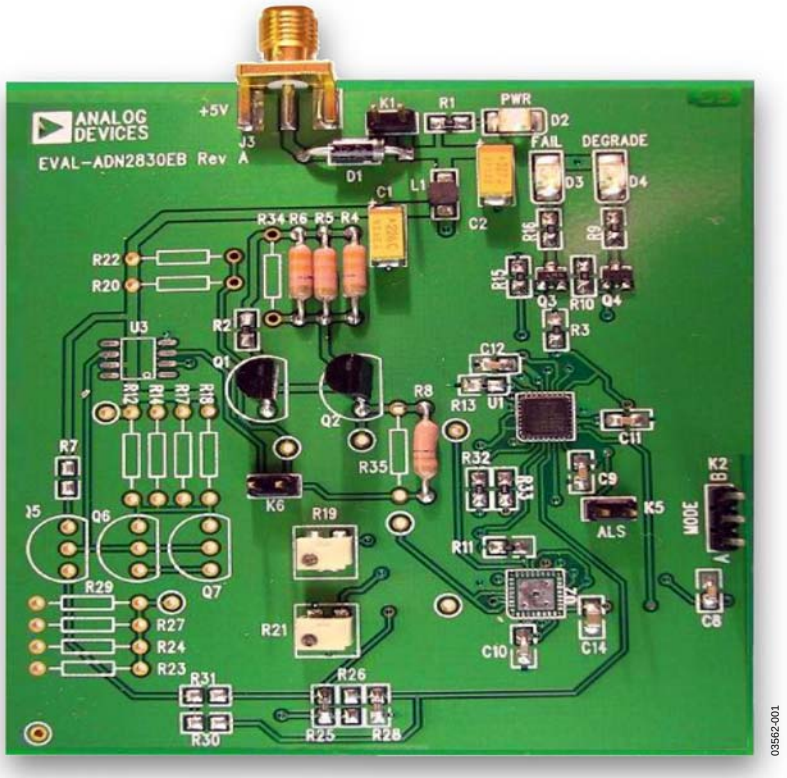

Figure 1.

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QUICK START GUIDE

Getting started with the ADN2830 evaluation board is a four-step process.

1. Set the bias to either current sink or current source mode.
2. Choose the current mirror gain.
3. Calculate the values for R19 and R21 (PSET and ASET).
4. Check the evaluation board and get started.

Setting the Bias

The ADN2830 evaluation board supports either of two working modes: current sink mode or current source mode. The factory default configuration is in current sink mode. The PNP current mirror (Q1 and Q2) is used to simulate a laser and an MPD. The mirror current gain relates to laser slope efficiency and MPD current. The current mirror has a default gain of 200; thus, the MPD current always equals the IBIAS current divided by 200.

To use the ADN2830 in current source mode:

- Populate the evaluation board with the U3, Q5, Q6, and Q7 components.
- Insert Component K6.
- Remove Resistors R8 and R35.
- Populate the board with R20 and R22.

The current sourced by Q6 and Q7 is given by the following formula:

$$I_S = I_{BIAS} \times \frac{R_{20} \,||\, R_{22}}{R_{12} \,||\, R_{14} \,||\, R_{17} \,||\, R_{18}} \quad (1)$$

where:
I_{BIAS} is the bias current provided by the ADN2830 (maximum 200 mA).
I_S is the source current required.

Connect Q5, Q6, and Q7 in a current mirror configuration to close the control loops. The gain of the mirror comes from the ratio (R12||R14||R17||R18)/R7. When choosing the components, avoid violating the IBIAS pin compliance voltage limitations as specified in the device data sheet.

Note that the current mirror circuitry does not simulate the laser threshold current.

Table 1. Board Settings Description

Component	Name	Default	Function
K1		Inserted	Jumper to bypass supply protection diode
K2	Mode	No	Obsolete in this kit version
K5	ALS	No	Jumper to exercise ALS (when inserted, the laser is turned off)
K6		No	Enables current sourcing circuitry when inserted
J3	Power	Inserted	5 V power input to the board
T1 and T2			Measure the BIAS current in current sinking mode
T3			Modulation current mirror monitor
T5 and T6			Measure the current provided by ADN2830 in current sourcing mode
T7 and T8			Measure the bias current in current sourcing mode
T13			IMPD current mirror monitor
R19			Set ADN2830 alarm current level
R21			Set bias current level

Choosing the Current Mirror Gain

When choosing the current mirror gain, it is important not to exceed 1.2 mA MPD current at the maximum bias current when using the IMPD block. When the anticipated MPD current is about to exceed 1.2 mA, the IMPD block may be bypassed and the control loop can be closed by connecting to the PSET node directly. This allows MPD currents as large as 8 mA.

Table 2. Using the IMPD Block

Configuration	R25/R31[1]	R26/R30[1]	R28
IMPD block used	Not populated	0 Ω	Not populated
Bypass IMPD	0 Ω	Not populated	0 Ω

[1] In sink current mode, R25 and R26 are used; in source current mode, R30 and R31 are used.

Calculating the Values for R19 and R21 (PSET and ASET)

The laser average power (IBIAS current) can be configured by adjusting the PSET potentiometer (R21). The average power control loop, which consists of a combination of internal and external circuits, sets the PSET pin to approximately 1.23 V. When using this evaluation board, it is easy to compute and program a desired value for IBIAS.

To calculate approximate values of R_{PSET} for a desired IBIAS

$$R_{PSET} = \frac{1.23\ V}{I_{BIAS} \times G} \quad (2)$$

where:
G is the current mirror gain.
$G_{sinking\ mode}$ equals $(R_{34}||R_5||R_4||R_6)/R_2$.
$G_{sourcing\ mode}$ equals $(R_{12}||R_{14}||R_{17}||R_{18})/R_7$.
R_{PSET} is the total resistance at the PSET pin (R21 + R33).

When using the evaluation board in current sourcing mode, the bias current from Equation 2 should be replaced with the sourcing current I_S as shown in Step 1 (Setting the Bias).

The alarm threshold level is adjustable by using R19. R19 is determined by

$$R_{19} = \frac{1.23\ V}{I_{fail}} \times 200 \quad (3)$$

where I_{fail} is the fail alarm threshold of the bias current. Any bias current higher than I_{fail} triggers the fail alarm.

In the current sourcing mode, calculate the bias current (the alarm threshold level) from I_S using Equation 1. The degrade alarm is raised when the bias current reaches 90% of I_{fail}. The total resistance at the ASET pin should be within the 1.2 kΩ to 13 kΩ range. Resistor R32 ensures that it will not short to ground. If the resistance exceeds 13 kΩ, the ADN2830 may not operate within specifications. The default values for Resitors R32 through R33 and Resistors R19 through R21 are 100 Ω and 50 kΩ. For high currents, it may be necessary to reduce these values to ensure accurate adjustments for the bias current and alarm threshold levels.

Note that when choosing the components from the current mirrors (resistors and transistors), it is important not to exceed the maximum power dissipation allowance set by the devices.

Checking the Evaluation Board and Getting Started

To check the evaluation board and get started testing the devices, follow the steps outlined below.

- Choose the jumper settings for the desired configuration (the default configuration is sinking current mode bypassing the IMPD block).
- Adjust R19 and R21 to the calculated values.
- Connect the power supply and adjust R21 in order to obtain the desired IBIAS current value.
- Ensure that the voltage at the cathode of D1 is within the range of 4.5 V to 5.5 V and then check the voltage compliance condition at the IBIAS pin ($1.2\ V < V_{IBIAS} < V_{CC}$). If one of these conditions is not met, the external circuitry should be redesigned. To do this, choose smaller values of degeneration resistors in the current mirror used.

The ADN2830 has fully integrated monitoring features of IBIAS and IMPD at the IBMON pin and the IMPDMON pin (T3 and T13, respectively). In current sourcing mode, take into account the ratio between the bias current given by ADN2830 and I_S when using the bias current monitoring function.

DESIGN EXAMPLES

When designing the external circuitry, it is important to establish the desired range for the bias current. If it is needed to use the IMPD block, carefully choose the current mirror gain to ensure that the IMPD current is within the 50 μA to 1200 μA range and the voltage on the IBIAS pin exceeds 1.2 V.

When the IMPD block is not used, there are no major restrictions in choosing the current mirror gain. Two design examples are available in this section. Although the current mirror gain used in these examples is 1/200, the gain can be changed to fit in other individual needs.

Current Sink Mode Design Example

Considering that the current mirror gain is equal to 1/200, the adjustable bias current can be:

- 10 mA to 200 mA when using the IMPD block.
- 4 mA to 200 mA (full range) when bypassing the IMPD block (connecting directly to P_{SET} node).

The lowest value of bias current achievable is determined by the minimum value of IMPD current and the current mirror gain (only when the IMPD block is used), and the highest value is limited by the ADN2830 (200 mA).

Assuming that Transistor $V_{BE} = 0.7$ V and $V_{IBIAS} = 2$ V (>1.2 V), then for the highest bias current (200 mA), use the following formula to calculate the values for the resistors from Q2's collector, R8 and R35:

$$(R_{34} \parallel R_5 \parallel R_4 \parallel R_6) + (R_8 \parallel R_{35}) = \frac{V_{CC} - V_{BE} - V_{IBIAS}}{I_{BIAS\,max}} = \frac{5 - 0.7 - 2}{0.2} = 11.5\ \Omega$$

where:
$R_{34}||R_4||R_5||R_6 = 10\ \Omega$ because R34 and R35 are not populated and $R_8 = 1$.

From the above derivation, one possible solution is $R_4 = R_5 = R_6 = 30\ \Omega$.

The current mirror gain is given by the following formula:

$$\frac{R_{34} \parallel R_5 \parallel R_4 \parallel R_6}{R_2} = \frac{1}{200}$$

As a result, $R_2 = 10\ \Omega \times 200 = 2$ kΩ.

R_{PSET} is given by the formula:

$$R_{PSET} = \frac{1.23\ V}{I_{MPD}}$$

$R_{PSETmin}$ is calculated when ADN2830 is sinking 200mA. Assuming that the current mirror provides 1 mA through R_{PSET} at the highest bias current, then $R_{PSETmin}$ = 1.2 kΩ.

The value for $R_{PSETmax}$ is

- $R_{PSETmax}$ = 1.23 V/0.05 mA = 24.6 kΩ, when the IMPD block is used.
- $R_{PSETmax}$ = 1.23 V/0.02 mA = 61.5 kΩ, when the IMPD block is bypassed.

As a result R21 = $R_{PSETmax}$ and R33=$R_{PSETmin}$. The mechanical trim pots used on this evaluation board are eleven-turn potentiometers. These potentiometers may limit the user's ability to fine tune the bias current. In practical applications, a digital potentiometer is recommended.

Current Source Mode Design Example

In this mode Q5, Q6, and Q7 work as a current mirror. The values of R7, R12, R14, R17, and R18 may be calculated in the same manner as in the previous example, considering the bias current as the current needed to be sourced. If the current sourced range is the same as the current sink range from the previous example, then R7 = R2, R5 = R4 = R3 = R12 = R14 = R17, and R18 are not populated. The current mirror gain gives the ratio between the MPD current and the current sourced.

With this assumption, at saturation $V_{CE} = V_{BE} = 0.7$ V, calculate the equivalent resistance connected to the collectors of Q6 and Q7 ($R_{29}||R_{27}||R_{24}||R_{23}$) using

$$(R_{29} \,||\, R_{27} \,||\, R_{24} \,||\, R_{23}) = \frac{V_{CC} - V_{CE} - I_{BIAS\max} \times (R_{12} \,||\, R_{14} \,||\, R_{17} \,||\, R_{18})}{I_{IBIAS\max}}$$

where $R_{29}||R_{27}||R_{24}||R_{23}$= 11.5 Ω
($R_{29} = R_{27} = R_{24} = R_{23}$ = 47 Ω).

Considering now the effect of the operational amplifier, the ratio between the sourced current and the bias current provided by ADN2830 is given by

$$\frac{I_{BIAS}}{I_{ADN\ 2830}} = \frac{R_{20} \,||\, R_{22}}{R_{12} \,||\, R_{14} \,||\, R_{17} \,||\, R_{18}}$$

Therefore, it is possible to source currents greater than 200 mA using only one ADN2830. Assuming that there is a 1:1 ratio between IBIAS and $I_{ADN2830}$, then R20=R22=20 Ω.

In both current sinking and sourcing modes, the alarm threshold is established by the resistor connected to the ASET node. The threshold represents the bias current value at which the fail alarm is raised. When the bias current reaches 90% of the threshold value, the degrade alarm is raised. In the sink current mode, the resistance needed to set the threshold is

$$R_{19} = \frac{1.23\ V}{I_{fail}} \times 200$$

where I_{fail} is the bias current provided by the ADN2830 which raises the fail alarm.

When the current source option is used, I_{fail} (from the previous formula) is obtained by multiplying the current sourced by Q6 and Q7 with the following ratio:

$$\frac{R_{12} \,||\, R_{14} \,||\, R_{17} \,||\, R_{18}}{R_{20} \,||\, R_{22}}$$

When choosing the resistors for the current mirror, consider that the resistors have to dissipate $P = I^2 \times R$ (maximum 0.4 W in these design examples). Also, consider that Q2, Q6, and Q7 should be able to provide the required current. The total power dissipated on these transistors should not exceed the transistor data sheet specifications.

$$P_{datasheet} > V_{cc\max} \times I_{C\max} / 4$$

where:
$P_{datasheet}$ is the power consumption specified in the data sheet.
V_{ccmax} is the maximum supply voltage.
I_{Cmax} is the maximum collector current required.

ADN2830 EVALUATION BOARD SCHEMATIC AND ARTWORK

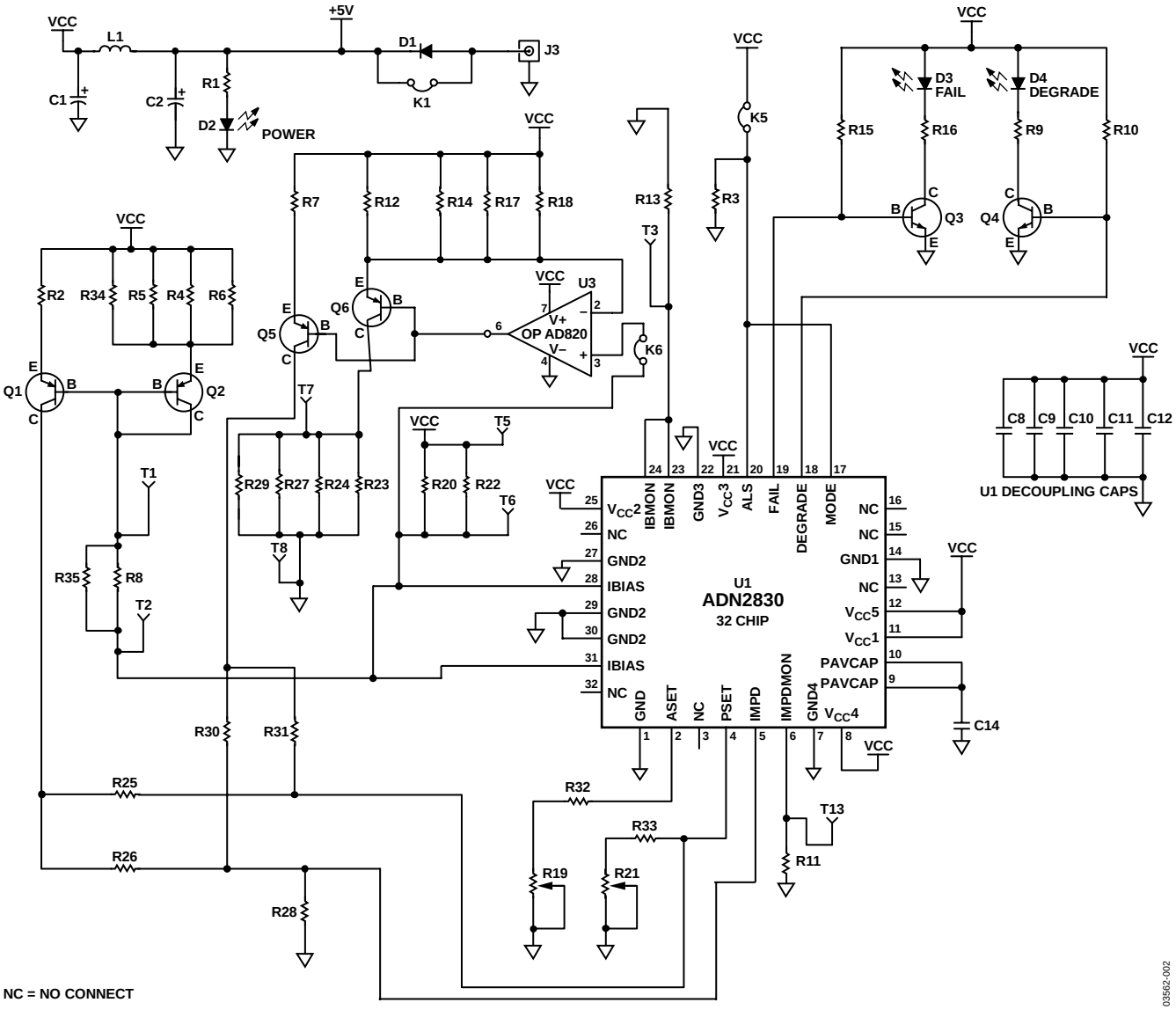

Figure 2. Schematic of the ADN2830 Evaluation Board

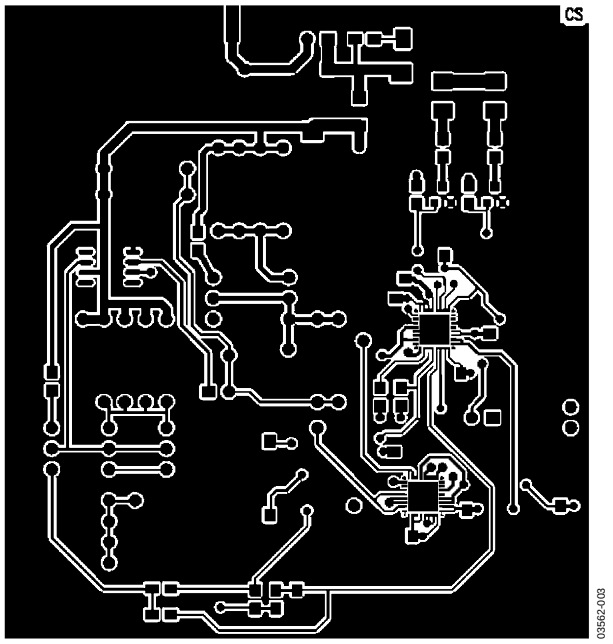

Figure 3. Printed Circuit Board Layout, Component Side

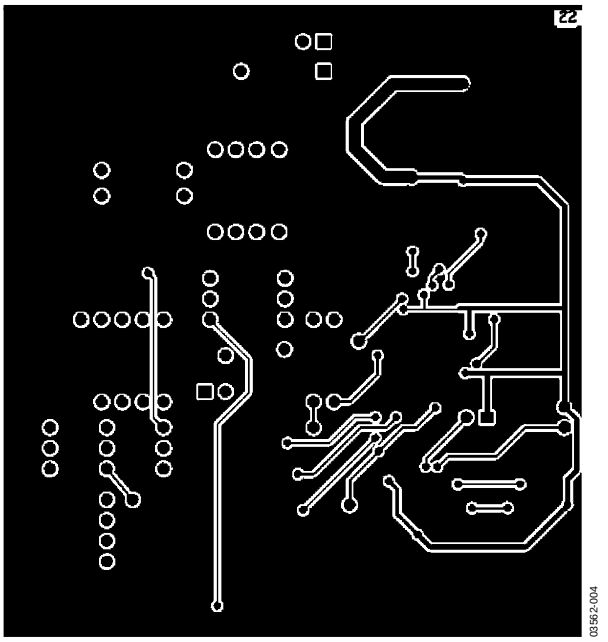

Figure 4. Printed Circuit Board Layout, Solder Side

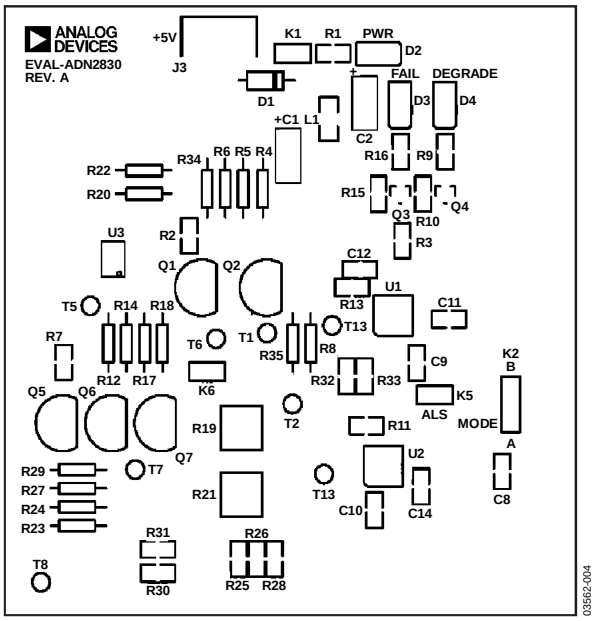

Figure 5. Silkscreen Image of the Evaluation Board

BILL OF MATERIALS

Table 3. ADN2830 Evaluation Board Bill of Materials

Quantity	Reference Designator	Value/Description	Populated?
3	R1, R9, R16	330 Ω, SMD 0603	Y
4	R3, R10, R11, R15	1 K Ω SMD 0603	Y
2	R19, R21	50 KΩ, SMD trim pots	Y
2	R32, R33	100 Ω, SMD 0603	N
1	R2	2.2 KΩ, SMD 0603	Y
3	R4, R5, R6	33 Ω, through hole	Y
1	R8	1.1 Ω, through hole	Y
2	R25, R28	0 Ω SMD 0603	Y
8	R20, R22, R23, R24, R26, R27, R29, R30	No specific recommendations	N
8	R7, R12, R14, R17, R18, R31, R34, R35	No specific recommendations	N
1	C1	22 µF SMD capacitor type C	Y
1	C2	220 µF SMD capacitor type C	Y
5	C8, C9, C10, C11, C12	10 nF SMD capacitor size 0603	Y
1	C14	1 µF SMD capacitor size 0805	Y
1	L1	10 µH SMD inductor size 1206	Y
3	K1, K3, K5	0.1" pitch, 2-pin header	Y
1	K2	0.1" pitch, 3-pin header	Y
1	K6	0.1" pitch, 2-pin header	N
1	J3	SMA side-launch connector	Y
1	D1	1N4001 diode plastic package	Y
3	D2, D3, D4	SMD LEDs	Y
2	Q3, Q4	SOT-23 transistors	Y
2	Q1, Q2	BC327	Y
3	Q5, Q6, Q7	BC327 (optional)	N
1	U1	ADN2830 32L LFCSP	Y
1	U3	AD820 SOIC	N

AN03562-0-11/07(A)