ANALOG DEVICES

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APPLICATION NOTE

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Operation and Applications of the AD654 IC V-to-F Converter*

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INTRODUCTION

DEVICE DESCRIPTION

The AD654 is a monolithic voltage-to-frequency (V/F) converter combining simplicity of use in standard applications with a high degree of flexibility and versatility. It is very much like its predecessor, the popular AD537.[1,2] The AD654 exchanges the all-around flexibility and versatility of the AD537 for maximum efficiency and economy of purpose, within a single 8-pin package. As a significant bonus, it adds an extended frequency range limit, contrasted to the original AD537.

Designed for either single or dual supply operation with low supply voltages and low current drain (5V and 1.5mA), the AD654 nevertheless has the capability of driving high voltage, high current loads (36V and 20mA). The chip includes a low drift input amplifier capable of operating directly from millivolt signals, a precision current controlled oscillator, and a high current output stage. It is a complete circuit, using low temperature coefficient silicon chromium thin-film resistors throughout. Only two application dependent external scaling/timing components are required; one resistor and one capacitor (Figure 1).

These two components provide the user with means for customizing the device for two application-unique parameters; scale of the input voltage and the output frequency. Programming of the full scale (FS) input voltage is possible from 100mV to 10V (or more, in some cases). The FS frequency can be programmed to any value less than 500kHz.

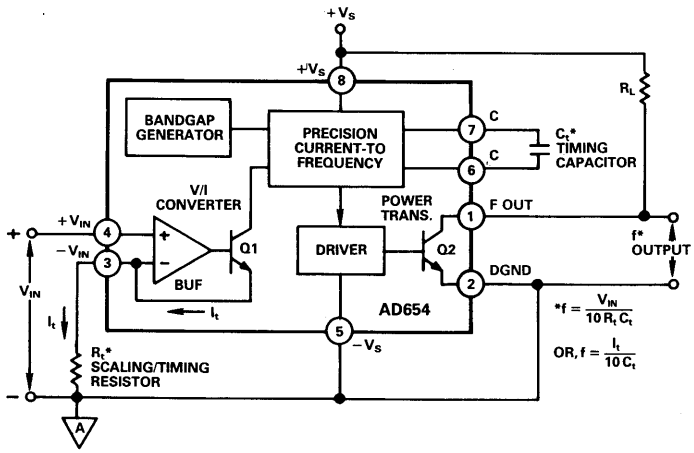
Either positive or negative input voltages can be accepted by the AD654 for a conversion. The basic AD654 V/F scaling relationship is:

$$f = \frac{V_{IN}}{10V \times (R_t C_t)} \qquad (1)$$

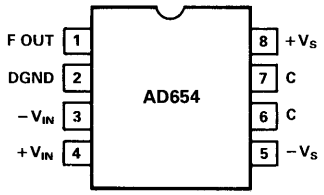
This simplifies the choice of the external components.

V/F linearity error is typically ±0.03% for 250kHz FS,

*Portions of this note are revised and expanded from the original "Applications of the AD537," by Barried Gilbert and Doug Grant.



a. Block Diagram



b. Schematic Symbol

Figure 1. AD654 Basics

guaranteed over an 80dB dynamic range. The output frequency is stable with temperature (typically ±50ppm/°C, excluding the effects of external components) and supply (typically ±0.05%/V from 5 to 36V). Complete specifications are included in the supplementary pages at the end of this note.

The input amplifier functions as a voltage-to-current converter and has a typical offset voltage drift of only ±4μV/°C. This low drift permits operation directly from such low level transducers as strain gauges, thermocouples, current shunts, etc, while offering a high (250MΩ) input resistance to positive voltage signals.

The output stage, an open collector NPN circuit, can sink up to 20mA with a saturation voltage less than 0.4V and can withstand a voltage of 36V. The collector and emitter

of this stage can be connected to any level between the limits of ground (or −Vs), and 4V below +Vs, permitting easy interfacing with any digital logic family. The high current capability means that LED's, long cables, or up to 12 TTL loads can be driven directly.

Unlike most V/F converters, the AD654 is designed to deliver a *square wave* output. This factor has advantages both internally and externally. Internally, it means that the power dissipation is essentially independent of frequency so that self-heating effects do not cause linearity errors. Externally, the average dc level of the output is constant, useful in ac coupled data links. It also allows direct operation as a phased-locked-loop within F-V circuits as well as other applications.

Whereas many V/F converters are limited in their range of applications to basic telemetry and slow A/D conversion, the low cost, low power drain, single-supply operation, and high operating speed of the AD654 open up a wide spectrum of uses.

THEORY OF OPERATION

The block diagram of the AD654 is shown in Figure 1. The key to accurate operation is the current-to-frequency converter, which is a very carefully designed multivibrator. The main advantages of this circuit are:

- Its simplicity—requiring a single timing capacitor,
- The use of push-pull charging—resulting in a large voltage across this capacitor, even at low supply voltages (for improved timing accuracy and low cycle-to-cycle jitter),
- Its square wave output—generally more useful than the narrow pulse generated by charge dispensing converters,
- Its high speed of operation—up to 500kHz, or higher with special operating modes,
- Its application flexibility, allowing cost-effective applications as well as high precision when needed,
- Its ability to operate from a single +5V power supply,
- And, most importantly, its good linearity.

By using special adaptive biasing techniques, operation of this multivibrator is possible over a very large dynamic range, from a maximum control current of 2mA to less than 100nA (a frequency range of 20,000/1 or more).

It can be shown that the basic circuit has a well defined temperature coefficient of 300ppm/°K at all values of control current. Use is made of the tight thermal coupling to the associated band-gap reference generator, which supplies an exactly proportioned temperature compensation voltage to the multivibrator. The band-gap cell also provides the required bias for internal operation of the chip.

The square wave output from the multivibrator operates the output drive circuit, which provides a floating drive current to the large geometry output transistor Q2 (Figure 1). Internally, there are actually two transistors in a thermally symmetric layout for minimal interaction with the remaining circuits. This transistor is designed for very low saturation voltage and is driven to combine low ON voltages with a well defined current limit.

A versatile operational amplifier serves as the input stage. Its purpose is to convert the applied input voltage to a proportional control current in Q1. This current is optimally 1mA at the input signal level corresponding to the maximum output frequency. With the internal strapping of Q1's emitter and the op amp's (−) input, the input voltage is effectively impressed across the user defined external scaling resistor (R_t) by the theory of zero input differential.

This resistor, R_t, is chosen to provide the needed transconductance for the application, consistent with the applied FS input voltage. For example, for a FS input voltage of 1.0V, the optimum resistor value is 1.0kΩ. The $+V_{IN}$ terminal of the op amp (pin 4) offers a high input resistance to the source, with a bias current of about 30nA. The design of this op amp ensures that the effect of finite bias current on drift is small. Drifts of the order of 4μV/°C can be achieved, even with source resistance/scaling resistance imbalances of 1k. Consequently, the AD654 can accommodate millivolt signals without the need for a preamplifier.

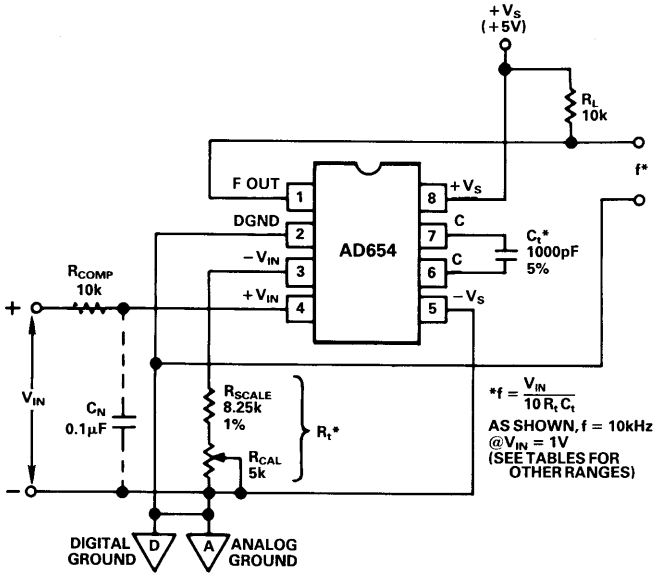
The input configuration is quasi-differential, so that errors due to ground loops can be avoided with the proper choice of signal connections. The common-mode range of the AD654 extends from 4V below $+V_S$ (that is, from +11V for a $+V_S$ of 15V), down to $-V_S$, so that inputs down to ground potential can be accepted even when operating from a single supply voltage. This feature maximizes the utility of the chip when operating from a battery or other single supply power source. Negative inputs (voltages or currents) can also be accepted by fixing the voltage on pin 4 (usually to ground potential) and driving a current into pin 3 (either directly from a current source, or via a scaling resistor).

Unlike the 14-pin AD537, the 8-pin packaged AD654 has no provision for trimming the offset voltage of the input op amp. However, since this error voltage is extremely low (1mV max), it is not likely to be a very significant factor in many applications. For example, even for an input FS voltage as low as 1V, this offset amounts to a zero error of only 0.1% of FS. For demanding applications, this residual offset can be trimmed externally at the option of the user.

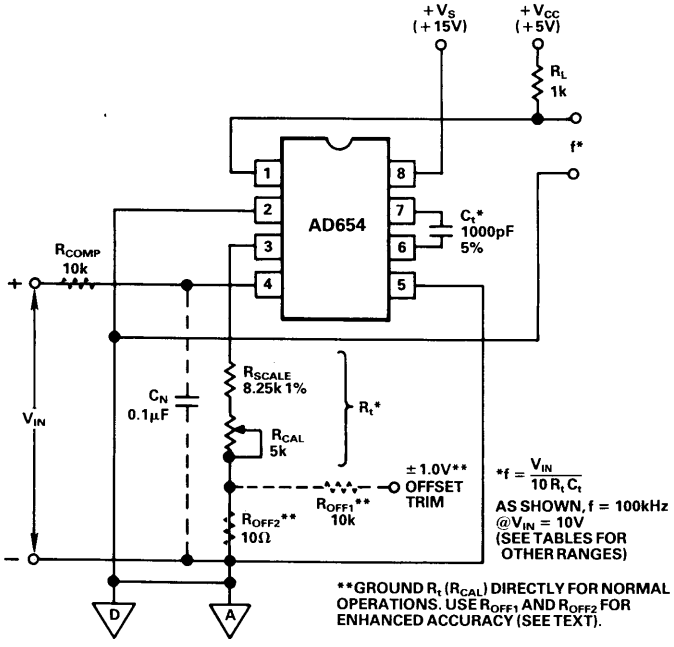
BASIC OPERATIONAL MODES

Positive Input Voltages

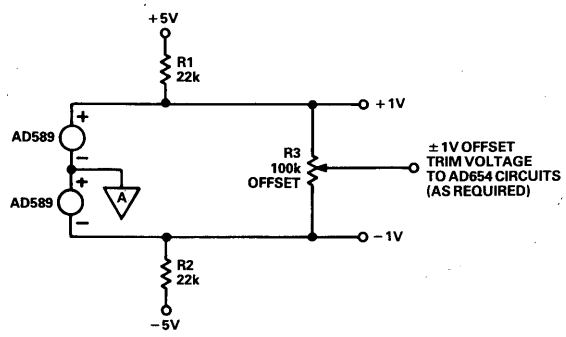
Figure 2 shows the connections for basic operation of the AD654 as a V/F converter with positive voltage inputs. For such operation, a single supply voltage will usually be sufficient, with $-V_S$ (pin 5) and the output emitter (pin 2) strapped to their respective grounds. The lower end of the scaling resistor R_t should be connected to the appropriate signal ground, shown here as *analog ground*. Note that this point is a noise-free, high quality ground, denoted by the "A" in the triangle. Note also that this point is common to the (–) side of the input signal, V_{IN}. This is to minimize conversion errors due to the inevitable voltage drops on PC board traces. The digital current path returns are denoted by the digital ground symbol ("D" in the triangle) and should be maintained separate from analog ground, except at one point. This convention is generally used throughout this note.



a. Low Power, 1V/10kHz



b. Wide Dynamic Range, 10V/100kHz



c. Offset Trim Bias Network

Figure 2. Basic Positive V_{IN} Connections

Choosing R_t and I_t

The nominal value of R_t is chosen for the application such that the FS input voltage sets up the desired FS current. There is a tremendous range of possible values here, due to the high dynamic range of the device. The designer can opt for a relatively low value of FS current I_t, and in so doing minimize the overall power consumption of the circuit. An example would be the use of a FS I_t of 100µA. Or operation can be towards a relatively high FS I_t of 1mA, whereby the maximum dynamic range and best linearity will be realized. It is the option of the designer to exploit this flexibility to the best advantage.

Since the input voltage V_{IN} appears across R_t, the relationship between R_t and I_t is simply:

$$R_t = \frac{V_{IN}}{I_t} \qquad (2)$$

Examples of standard operation are contained in Table I, but are discussed here to bring out the "why".

For a 0 to +1V input, where power is to be conserved, the circuit of Figure 2a is appropriate. This is a 10kHz FS circuit operating from a 5V supply. To minimize current drain, I_t is set at 100µA FS by the choice of R_t. R_t is nominally 10k for a 100µA FS current with a 1V V_{IN}. This is noted in the left column. It is a simple matter to recalculate R_t for other FS input voltages and/or currents not contained in the table. For example, for a max V_{IN} of 0.5V, R_t would be 5k for the same I_t. In the interest of simplicity, however, Table I summarizes the most useful operating ranges of the AD654 in terms of FS voltage, FS current, and the appropriate R_t value.

FS frequency is programmed via the choice of C_t, which is discussed latter. The circuit of Figure 2a is useful when overall simplicity is important and a three decade or lower dynamic range is adequate. The next example is slightly more complex, but realizes more dynamic range and higher speed.

FS V_{IN}	R_t FS I_t = 100µA	R_t FS I_t = 1mA
100V*	1 meg	100k
10V	100k	10k
1V	10k	1k
100mV	1k	100Ω

NOTE
*Applies *only* to Figure 3.

Table I. R_t Selection for V_{IN}; I_t

For applications requiring higher speed or the maximum dynamic range of the AD654 the circuit in Figure 2b is a good choice. This is for a 0 to +10V input, with R_t nominally 10k for a 1mA FS operating current; the FS frequency is 100kHz. This V/F operates from a 15V supply because of the 10V range. Other values of R_t can be selected as noted in Table I. R_t can be recalculated for any intermediate FS input voltage.

When operating in this general mode of input, it is important to note that the maximum allowable voltage input range of the AD654 is limited by the power supply voltage. For example, with $+V_S$ at 5V (as in Figure 2a) the maximum signal input is only +1V ($+V_S - 4V$). However, the device specifications do allow for the fact that the supply may be 10% low. In practice, reliable operation can actually be achieved for actual inputs slightly in excess of +1V with a 5V supply. By the same token, to accommodate an input voltage range of +10V, the $+V_S$ supply must be at least +14V ($+V_{IN} + 4V$), as in Figure 2b. Therefore, using a 15V supply a 10% input over range is possible.

Choosing C_t

Having chosen the input scaling resistor and I_t to fit the general requirements, the timing capacitor C_t is then selected. Note that C_t is chosen to accommodate the desired FS frequency, *after* R_t and I_t have been established. The basic relationship of (1) can be re-written in terms of C_t, as:

$$C_t = \frac{V_{IN}}{10R_t f} \qquad (3)$$

Or, since V_{IN}/R_t is equal to I_t, this expression can be also be written in an alternate form, as:

$$C_t = \frac{I_t}{10f} \qquad (4)$$

Equation 3 can be used to verify the values of the example(s). In the example of Figure 2a, with V_{IN} FS = 1V and R_t = 10k, the value of C_t will be 1000pF for a FS frequency of 10kHz. This can also be noted from the information of Table II (left column, bottom).

The scaling of a V/F is often specified in terms of conversion *sensitivity*, i.e., in Hz/V. In this case the scaling is 10Hz/mV. Table II simplifies the selection of C_t, allowing easy choice as is appropriate to FS frequencies of up to 500kHz. Higher frequencies are also possible, as noted. However, some special constraints are applicable, and are covered with the applications section.

For the 10V FS input voltage example of Figure 2b (again with R_t = 10k nominal, but I_t = 1mA), the value of C_t will be 1000pF for a FS frequency of 100kHz. This can also be noted from the information of Table II (right column). The scaling in this case is again 10Hz/mV.

Note that generally one must select the 1mA current ranges of I_t for the highest frequency ranges. This is to maintain optimum operating speed within the device. Additionally, when operating above 10kHz the value of the load resistor, R_L, should be lowered to minimize delay due to the associated time constant. A value of 1–2 kilohms is appropriate for the highest ranges, asshown in Figure 2b. At FS frequencies of 10kHz or below these measures are not neccessary and power can be conserved by operating at an I_t of 100μA, as in Figure 2a.

FS f	C_t FS I_t = 100μA	C_t FS I_t = 1mA
≥1MHz**	*	≤100pF**
500kHz	*	200pF
250kHz	*	390pF
100kHz	*	1000pF
10kHz	1000pF	10000pF

Notes
*Not recommended, see text.
**"Exalted" operation, see text.

Table II. C_t Selection for FS f; I_t

In general, the recommended C_t values are the most readily available ones. Within limits, any convenient value can be used to set up a special scaling relationship with some additional caveats. Linearity will be degraded with capacitor values below 1000pF, and 100pF is the minimum generally recommended capacitor size. There is no theoretical upper limit, but in practice there is a real one (see the section "Timing Component Selection").

Bias Compensation

In terms of optimizing the interface presented to the signal source, there are only a couple of considerations necessary. Since the input resistance at pin 4 is very high, errors due to non-zero source resistance will not normally be a serious problem. The low input bias current (30nA, typ) will generate an offset voltage of 30μV/k of *differential* source resistance. From this viewpoint, it is then desirable to keep the dc source resistances seen by the two inputs as near equal as is practical to minimize this error.

Generally speaking, bias current compensation resistance can be added to the inputs to minimize the resistance difference. However, with the AD654 it can only be added to the op amp's (+) input; that is, in series with pin 4. The resistance at the (−) input (pin 3) will simply be the value of R_t, and cannot be compensated without upsetting the scaling. Thus, minimizing bias current error will amount to keeping the total dc resistance seen at pin 4 as near equal to that at pin 3 by adding a padding resistance when appropriate.

An example of such a resistance can be seen in Figures 2a and 2b as R_{COMP}, the same value as R_t. The use of R_{COMP} is suggested for any applications where low end dynamic range is important (that is below a few mV), and in particular when R_t is 10k or more. Note that this resistance can also serve as the "R" section of an RC low-pass filter in conjunction with C_N. This filter is recommended to minimize noise disturbance of the V/F at low levels. C_N is not highly critical and can be chosen with this resistor for up to a 100ms time constant for maximum filtering. In general, a small value will also be effective (~0.1μF).

Calibration

In theory, two adjustments are necessary for the calibration of a V/F; FS (full scale) and ZERO scale (offset). In practice, the offset voltage of the AD654 is sufficiently low

that in many cases its adjustment is simply not necessary. If the very best low end accuracy is required, the device can be offset trimmed as follows. Note that the dynamic range of the lowest ranges (100-200mV) will be essentially determined by offset voltage limitations, not current related ones.

When offset voltage is to be trimmed, the trim will be done *external* to the device using an optional connection, such as that shown in Figure 2b. Resistors R_{OFF1} and R_{OFF2} are additional standard resistors placed to add a variable offset in series with R_t. A variable source of ±1.0V is applied to R_{OFF1} to adjust the offset as much as ±1mV. A simple bipolar source of ±1.0V could be two AD589's connected as shown in Figure 2c or a pair of LED's where the high stability of the AD589's is not necessary.

For most applications of the AD654 the major calibration trim will be for FS, which considerably simplifies its setup. In general, FS trim is the calibration of the circuit so that it produces the desired output frequency with a FS signal input. Specifically, this is accomplished by adjustment of the scaling resistor R_t, in most cases. The precise calibration of an AD654 requires the use of an accurate voltage standard set to the desired FS value and an accurate frequency meter, while a scope is useful for monitoring the output waveshape. Verification of converter linearity requires the use of a switchable voltage source or DAC having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Since each AD654 is factory tested for linearity, it will not usually be necessary for the end user to perform this tedious and time consuming test on a routine basis.

In application circuits, sufficient FS calibration trim range must be provided to accommodate the worst case sum of all major scaling errors. This includes the AD654 full scale error (±10%), the tolerance of the fixed timing resistor (±1% assumed), and the tolerance on the timing capacitor (±5% is assumed). Therefore, in these discussions a trim range of ±16% will be used, since this will accommodate all of the above. In the circuit examples, the fixed part of R_t will be 82% of the nominal, and the variable portion chosen to allow 116% of nominal.

For instance, this would be an 8.25k ±1%, ≤100ppm/°C metal film resistor for R_{SCALE}, plus a 5k trimmer for R_{CAL}, for a net R_t of 10k. For the adjustable portion, this should be an infinite resolution film trimmer, with high mechanical stability and low TC (≤100ppm/°C), sealed against the environment. For other values of R_t, use the same general proportions.

Although device warmup drifts are small, it is always good practice to allow the circuit's operating environment to stabilize before trim, and to provide the pertinent supply, source and load conditions. The calibration is begun with the offset trim (if applicable). If no provision is made for offset trim (or it is not neccessary to the application), proceed to FS calibration.

ZERO (Offset) Calibration

For ZERO scale cal, accomplished by offset trimming, begin by setting the input signal voltage to zero by shorting the inputs. Adjust the offset pot until the AD654 just ceases to oscillate. This may be most easily seen using a scope at the output; the adjustment required should be slight. At this point, the device should already be close to calibration at low scale. Apply a known source of 1mV to the V/F input and adjust the offset trimmer further for the correct output according to Table III. For example, if the FS V_{IN} is 1V and the FS frequency is 10kHz then the offset trim frequency will be 10Hz (Table III, left column). Note also that this adjustment will be quite tedious unless the counter is used in the PERIOD mode, adjusting for 0.1S.

With offset properly adjusted, proceed with FS calibration, as follows:

FS Calibration

To trim an AD654 for a desired FS frequency, apply a known FS input voltage at the appropriate level and adjust the R_{CAL} portion of R_t until the desired FS output frequency is indicated on the counter (Table III). In some applications where the FS input voltage is small (≃100mV) this adjustment may slightly affect the device offset voltage due to the presence of bias current at pin 3.

In a case where the offset is being trimmed and where the highest accuracy is desired, it may be appropriate to repeat the ZERO and FS adjustments until no further improvement is possible. If offset is not being trimmed, the FS adjustment completes the converter's calibration.

	FS Frequency		
FS V_{IN}	10kHz	100kHz	500kHz
10V	10V → 10kHz 1mV → 1Hz	10V → 100kHz 1mV → 10Hz	10V → 500kHz** 1mV → 50Hz*
1V	1V → 10kHz 1mV → 10Hz	1V → 100kHz 1mV → 100Hz	1V → 500kHz** 1mV → 500Hz*
100mV	100mV → 10kHz 1mV → 100Hz	100mV → 100kHz 1mV → 1kHz	100mV → 500kHz** 1mV → 5kHz*

Notes
*Adjust OFFSET (if used) as noted.
**Adjust FS cal as noted.

Table III. Calibration Tables for Various Ranges

Negative Input Voltage

By interchanging the two input connections the AD654 can operate from negative input voltages, as shown in Figure 3. In contrast to the connections of Figure 2, this circuit does *not* offer a high input resistance since the entire control current must now be provided by the source. Consequently the input resistance is simply equal to the scaling resistance R_t which is again chosen to set up a desired I_t at the FS input voltage in use. In this example, a −10V V_{IN} is used with a 5V supply and the FS frequency is 10kHz. Note that other values of R_t can be selected from Table I.

In this case, the FS voltage can now be as large as desired since it is limited neither by the input amplifier common mode range, nor by the supply voltage. For example, a −100V FS input would use a scaling resistor of 100k, and the AD654 could still operate from a +5V supply in the circuit as shown, with only this single change.

If it is desirable to reduce both power consumption as well as the loading on the signal, a lower FS I_t can be used. For example, a 1MΩ resistor could be used for R_t to convert

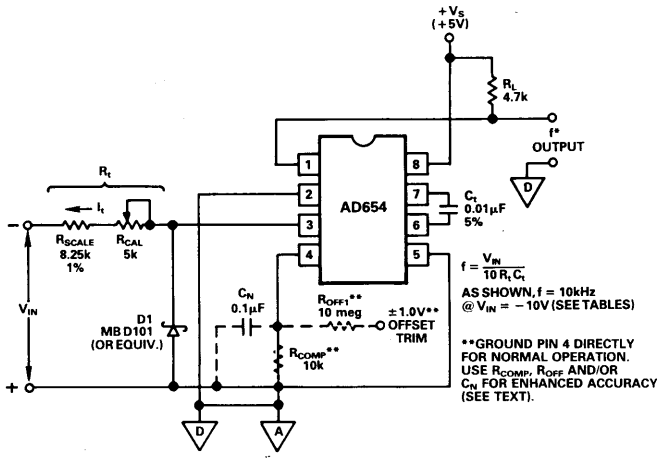


Figure 3. Negative V_{IN} Connection, −10V/10kHz

the −100V input into a 100μA FS I_t as noted in Table I. For the same FS frequency (such as 10kHz in this example) the timing capacitor would then be reduced by a factor of ten, and would be 1000pF (Table II). The same general considerations apply to this circuit with reference to speed as were applicable to the circuits of Figure 2.

A point worth noting is that when lower values of I_t are used, not only is power conserved, but a very large input over-range capacity is also provided (20/1 at I_t = 100μA). This can be useful in handling signals which may occasionally have large peak values.

When operating in this general mode, pin 4 will usually be at ground potential or the signal return level. This results in a current summing node at pin 3. Thus, any number of signals may be algebraically added before conversion and each source may have any desired scaling by appropriate choice of the associated resistor. Note however that it is not fundamentally necessary for pin 4 to be grounded; in fact offset scales can be generated by setting the voltage on this pin to some (stable) level.

For lowest offset voltage error, the optional compensation resistor (R_{COMP}) can be added at pin 4 in lieu of grounding the pin directly. This is not likely to be necessary except on the very lowest voltage scales or with high values of R_t (above 10kΩ). If offset is to be trimmed, one more resistor is added, R_{OFF}. This is selected to provide a ±1mV range at pin 4, with ±1.0V input. If a resistor is used for R_{COMP}, it may lead to noise coupling at pin 4. It should be bypassed for lowest noise, particularly in the higher values, with a capacitor such as C_N.

At any time when the inputs of the AD654 are operated from a negative source, it is imperative that the designer control the potentials at pins 3 and 4 with respect to −Vs (pin 5). *Neither input should be allowed to see voltages of more than −300mV with respect to pin 5.* If such a condition should occur, unpredictable behaviour of the V/F may result, and latchup may occur. With this in mind, the source to be used should be tested thoroughly for any possible over-range transients which could give rise to such input conditions. In the event that transient behaviour cannot be totally characterized as safe, a protective clamp diode can be used. This clamp, D1 in Figure 3, is a low leakage type with a low forward threshold and will provide adequate overload and latchup protection when located *after* R_t, as shown.

For applications where the best possible linearity performance is important, it is worth noting that the linearity in the negative input mode as shown here is inherently better than for the positive voltage mode circuits of Figure 2. This comes about since the degrading effect of finite common-mode rejection inherent to that connection is eliminated. It also allows the use of the minimum supply voltage.

The design considerations and trimming procedures for this circuit are otherwise the same as for the positive input voltage mode. Similar allowances for component tolerances should be provided and stable components used when requirements so dictate.

Negative Input Current

In some cases the input signal may be in the form of a negative *current source*. True current sources can be handled in a way somewhat similar to negative input voltages. However, the scaling resistor is no longer required, eliminating the capability of trimming the FS frequency in this fashion. In fact, trimming presents some special problems when the signal input is a true current source.

Operating the AD654 in a current input mode results in the slightly modified transfer expression:

$$f = \frac{I_t}{10C_t} \qquad (4)$$

As equation (4) states, the output frequency is only dependent on two variables, I_t (the input current to pin 3) and C_t. Since it will not always be practical to smoothly vary the capacitance for calibration purposes, an alternative scheme is needed.

A basic V/F circuit suitable for operation from a current source with a FS level of 1mA is shown in Figure 4. In operation, this circuit divides the input current into two main paths. One path is through the 100Ω resistor R1, and flowing into pin 3; it constitutes the signal current I_t to be converted. The second path, through another 100Ω resistor R2, carries the same nominal current. Two equal valued resistors offer the best overall stability, and should be either 1% discrete film units, or a pair from a common array.

As a result of the above, the 1mA input current is divided into two 500μA legs, one to ground, and one into pin 3 of the AD654. Since the total input signal current (I_s) is divided by a factor of 2 in this network, C_t must be reduced by a factor of 2. This results in a new transfer expression unique to this hookup:

$$f = \frac{I_s}{20C_t} \qquad (5)$$

As can be noted from the circuit values, a 5000pF capacitor will provide a FS frequency of 10kHz with a signal input (I_s) of 1mA.

For calibration purposes, resistors R3 and R4 are added to the network, allowing a ±16% trim of scale factor with the values shown. This will allow resistor-only trim for

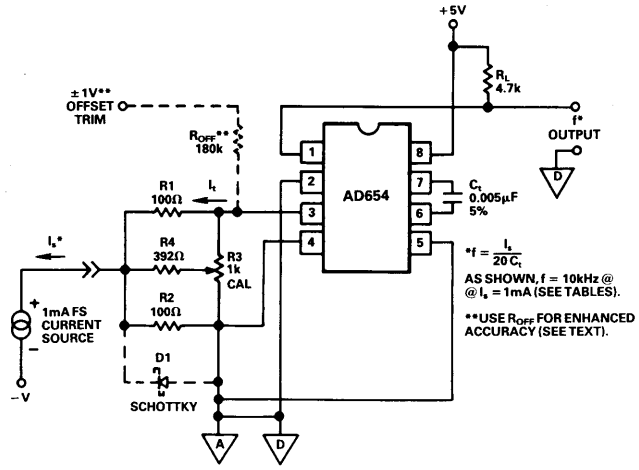


Figure 4. Current Source Input Connection

calibration of all the tolerances previously discussed. If the trimming range needs modification, R4's value can be changed. For example, a current output device such as a temperature transducer will typically have a specified calibration tolerance, and R4 can be lowered to accommodate this range.

For the greatest V/F dynamic range, some consideration to offset voltage should be given when using this circuit. Because of the current fork input network, a finite voltage offset in the AD654 can actually result in low frequency oscillation *without* a signal present! This will be understood when the paths for offset voltage induced parasitic currents are considered. Practically, the solution to minimizing this problem is to use an offset null externally. The optional input shown with the use of R_{OFF} will accommodate ±1mV of device offset.

Care must be taken when dealing with negative current inputs to this circuit for the same general reasons as outlined above under negative voltage inputs. Again, pins 3 and 4 must *not* be allowed to see more than −300mV with respect to pin 5. In this circuit, the low values of R1 and R2 prevent this for normal operation (plus some overrange). However, if transient currents can produce dangerous voltages, the use of a Schottky clamp diode is recommended.

The values of R1-R4 shown are suitable *only* for 1mA sources, but they can readily be scaled upward (proportionally) for lower FS current levels. For example, if one had a 100μA source signal these resistors would be increased by a factor of ten. At a given FS input current the R1-R2 junction should operate at about −50mV. The values of these resistors should never be set to allow more than 100mV drop under maximum input conditions.

Some General Precautions and Housekeeping

The AD654 is intended to be used with a minimum of additional hardware and the circuits shown in these notes are for the most part complete. However, the successful application of any IC involves a good understanding of all possible pitfalls, and the use of suitable precautions and preventions.

Input Protection

In general, pins 3 and 4 of the AD654 should never be driven more than 300mV below $-V_S$ (pin 5). If done, this could cause internal junctions to conduct, possibly damaging the IC or causing latchup. The AD654 can be protected from "below $-V_S$" inputs by suitable choice of input resistance and a clamping diode, as discussed in the basic applications section. The most important requirement of this clamp is that it must have a low forward threshold, ie., 300mV. A Shottky type is generally recommended in the figures. In some instances, where the higher leakage may be not be a factor, germanium types may also be useful, such as 1N67, 1N270, etc.

It is also desirable not to drive pins 3 or 4 *above* $+V_S$. In operation, the converter will become very nonlinear for voltage inputs above $(+V_S - 4.0V)$. Input control currents above 2mA will also increase nonlinearity. By carefully designing for operation within the device's recommended limits, the user will avoid these "murky" areas and assure the possible highest performance.

Noise Filtering

The full rated 80dB dynamic range of the AD654 is for operation from a control current of 1mA (nominal FS) down to 100nA (this is equivalent to a 1mV input for 10V FS). For I_t below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases, this phenomenon might be due to short duration noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, −80dB is a voltage of only 100μV. For the same scale, a mean input of −60dB is 1mV and noise spikes of only 0.9mV are sufficient to cause momentary malfunction.

This particular problem can be minimized by using a simple low pass filter ahead of the converter. In fact, in *any* case where low scale operation is expected, filtering/bypassing around the inputs is recommended. For a FS of 10kHz, a single pole filter with a time constant of 100ms will be suitable. As noted in the examples, this resistor can also serve as a bias compensation resistance, enhancing accuracy there as well. Note that filtering within the signal path is also applicable to the negative input voltage mode, simply by splitting R_t into two parts with the midpoint bypassed by a capacitor to analog ground.

Of course, the optimum filtering configuration will depend on the application and the type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time. Above 100nA (1mV) inputs, full integration of additive input noise occurs.

The AD654 is somewhat susceptible to interference from other external signals. The most sensitive nodes (besides the inputs) are the capacitor terminals. The timing capacitor should be located as close as possible to the AD654 package to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. Of these two precautions, guarding is the easier to implement as the package layout normally will guard pins 6-7 with pin 5 grounded and pin 8 to $+V_S$ (ac ground).

The latter technique (shielding) is not likely to be necessary except with the use of higher value film capacitors which can be quite large physically. It is usually desirable to minimize capacitor size, not only from a noise susceptibility point of view, but also from a cost standpoint.

Decoupling

It is generally good engineering practice to use bypass capacitors on the device supply voltage pins and to insert small valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. For local bypasses at the IC terminals, ceramic, stacked film, or other comparably low-inductance capacitors in the 0.1μF to 1.0μF range are recommended in parallel with a low ESR electrolytic capacitor (0.1Ω or less at 100kHz). Note also that three terminal regulators are excellent spot decouplers and available in high performance-for-cost TO-92 packages.

Finally, it should be understood that proper attention to grounding at the analog and digital common points is a large part of successful operation of AD654 circuits. The digital and analog grounds should be connected at a single point to minimize the cross-coupling of currents and spurious error voltages. The floating output structure of the device goes a long way towards this but careful wiring should always be done, particularly where the accuracy required is high.

TIMING COMPONENT CONSIDERATIONS

Temperature Stability

The stability of the AD654's output frequency is determined by several factors. Broadly speaking, they can be grouped into offset drift and scale drift, or the TC of these parameters. Fortunately, the design of the AD654 is such that the amplifier's input offset drift is very small (in the 4μV/°C region). Unless the circuit is to be connected for operation from very low signal levels, this will rarely be a significant source of instability.

Temperature induced changes in the conversion scale factor include sources of more serious error. Scaling drifts arise both in the AD654 itself and in the external timing resistor and capacitor. Inasmuch as the AD654 commercial temperature range scale drift is typically ±50ppm/°C, the external timing components can in many cases contribute larger TC's. Both R_t and C_t should be selected for a quality consistent to the particular application. In practice, it is more likely to be the external R_t and C_t components which most seriously degrade stability over temperature, particularly the capacitors.

The best choice for a timing capacitor is dependent on a number of parallel performance considerations and of course, cost. As always, careful tradeoffs should be made to match the best performance parameters to the particular application. This is especially true for timing components used with the AD654.

Good V/F linearity definitely requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small temperature coefficient. NPO ceramic, polypropylene, Teflon, and polystyrene capacitors as a rule best serve these two needs. These types should be the components of first choice. Mica and polycarbonate dielectrics are less desirable due to linearity degradation. Linearity and stability are generally degraded with most other types. Capacitor *tolerance* is not a major factor since it should be trimmed out as part of the calibration. 5% units are assumed for these applications.

Polystyrene types have very low DA and reasonably low TC (typically $\simeq -120$ppm/°C, this varies somewhat with processing), low cost, and reasonable size. The TC of polystyrene is also very *linear*, allowing compensation with a positive TC resistor. Polypropylene is similar, but with a wider range of values. Film types such as polypropylene are available in values up to 10μF or more. Teflon is superior in almost all regards (except cost), and will be unmatched for operation over 100°C. "NPO" or "COG" characteristic ceramic capacitors are the most desirable from the mutual standpoints of size, low TC (nominally zero), and a reasonably low DA. While the DA of this type is not as low as the better films (and it is not manufacturer controlled . . . a potential caveat), is still low enough to be very effective, particularly where the lowest TC is of paramount importance. Any other ceramic type should be avoided for timing uses.

For the scaling/timing resistor, the selection problem is much less severe. For most applications, metal film resistors are recommended, as they are available off the shelf in a wide range of values, and with TC's down to 50ppm/°C (or less).

In any event, when the lowest temperature errors are required of an AD654 circuit, care should be taken to minimize unnecessary heat sources, and keep all temperature sensitive components in close proximity to one another. For the most critical applications, RC components with nominally zero or the lowest available TC's can be used. This would suggest 25 or 50ppm/°C film resistances, and COG ceramic capacitors, which will minimize the timing component error. The ultimate in TC performance can be achieved only through rigorous attention to all temperature related factors. Application examples will illustrate this.

Other Capacitor Considerations

Since the voltage on the AD654's capacitor reverses polarity every half cycle, nonpolarized types must be employed. For use at very low FS frequencies, this becomes a problem in terms of both size and cost. This will generally rule out electrolytic types for precision applications.

As a practical note, if the maximum V/F dynamic range is not absolutely necessary to a given application, the capacitor size can be minimized by operating with a reduced FS current (rather than 1mA). For example, a 10/1 increase in R_t will reduce this current and allow a 10/1 reduction in C_t for the same FS frequency. Tables I and II will be helpful in making this type of tradeoff.

Output Interfacing

The AD654's logic output stage, available at pins 1-2, is designed to interface easily with all digital logic families. This includes LED's (for optical coupling), pulse transformers, and long lines. Due to the internal floating drive scheme, both the collector (1) and the emitter (2) of the stage's NPN transistor are available for external discretionary uses. The emitter can be tied to any potential from ($+V_S$–4V) down to $-V_S$, and the collector can be pulled up to 36V above the emitter (regardless of the $+V_S$ level applied to pin 8).

Logic Driving

Figure 5a shows the AD654 connected for a 0 to +10V voltage input with general output interfacing. The required logic common voltage (V_{EE}), the logic supply voltage (V_{CC}), the pull up resistor (R_L), and the $-V_S$ supply for the AD654 are shown in the accompanying table. The user can design an appropriate interface by selecting the proper set of conditions from this table. In the TTL mode, up to 12 standard gates (20mA) can be driven at a maximum LOW state voltage of 0.4V. This output flexibility is available with all the other possible input connections not explicitly shown.

The AD654 output stage is current limited, and the collector node (pin 1) can be shorted indefinitely to pin 2 (normally logic ground). When this point is shorted to $+V_S$, the current in the ON state (if not limited by any external means) will be approximately 35mA. Under most conditions this will not result in damage.

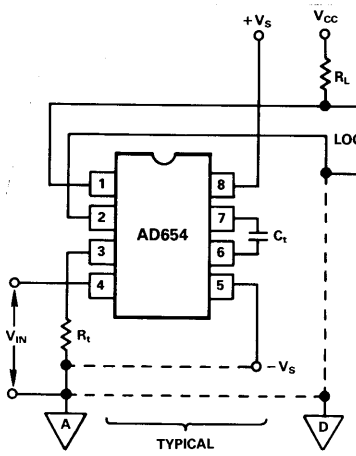
As an example, with pin 2 grounded, pin 1 shorted to +15V, and the oscillator running, the average power in the output stage is 262.5mW (15V × 35/2 mA; at a 5V supply it will be 1/3 this power). If however, a high supply voltage is used on the logic stage and the output is in the ON state for long periods (i.e., at a low frequency/long period), the peak dissipation of 1260mW (36 × 35) will cause considerable heating. It is recommended that this situation be avoided for prolonged periods of time, particularly with the plastic package device.

While the AD654 has ample drive for lower frequency TTL loads, at frequencies above a few hundred kHz it can begin to lose square wave symmetry and logic saturation. For operation above 200kHz into TTL or other logic type loads a buffer is recommended, as shown in Figure 5b.

Phantom Power Schemes

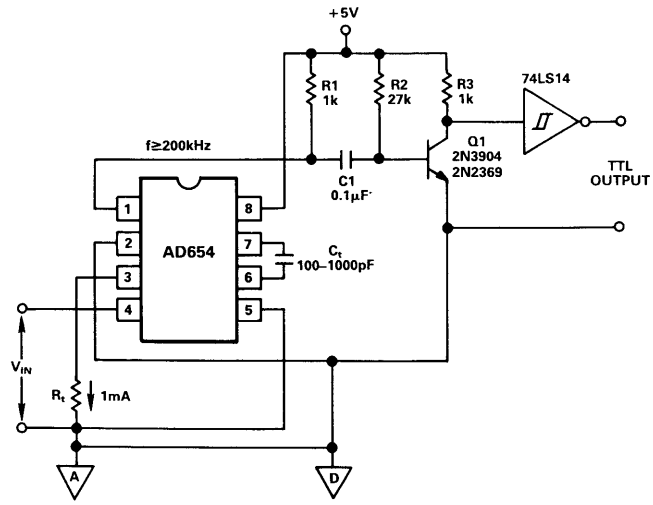
It is very often desirable to power a remotely located V/F circuit via a simple cable hookup while taking the output signal from the same cable. Whenever possible, it is also useful to use the most simple cabling, such as a plain #22 twisted pair. Concurrent power/signal transmission on the same cable implies suitable separation circuitry so that no loss of performance results. Two circuits suitable for phantom power of AD654 V/F converters are shown in Figure 6.

Figure 6a is a simple but effective hookup useful for interfacing with a variety of logic types at the output. The positive supply line is fed to the remote V/F cable through R1.



	V_{CC}	V_{EE}	R_L	$-V_S$
TTL/LSTTL	+5	GND	4.7k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS	+15	GND	10k	GND

a. Standard Interfacing



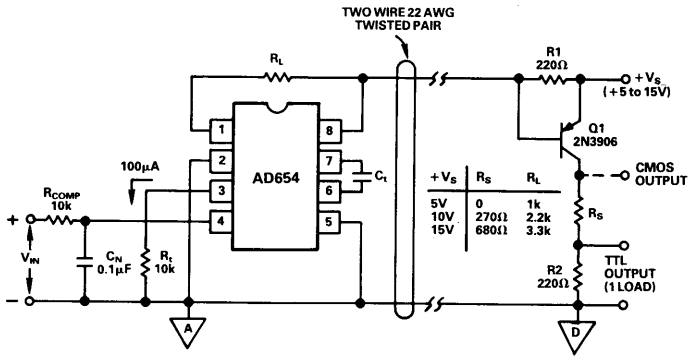
b. High-Speed TTL Output Buffer

Figure 5. Interfacing with Standard Logic

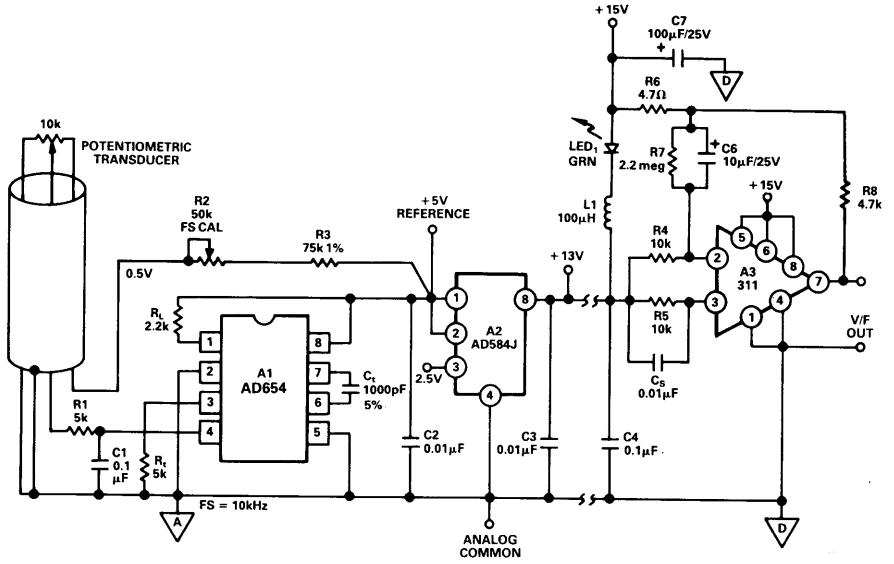
This resistor is selected such that the quiescent current of the AD654 will cause less than one V_{BE} to be dropped. As the V/F oscillates, additional switched current is drawn through R_L at pin 1. The peak level of this additional current causes Q1 to saturate, and thus regenerates the AD654's output square wave at the collector. In the process of supplying power to the AD654, the supply voltage is reduced one V_{BE} plus the line drop.

To set up the receiver circuit for a given voltage the R_S and R_L resistances are selected as appropriate from the table. CMOS logic stages can be driven directly from the collector of Q1 for any supply level. A single TTL load can be driven from the junction of R_S and R2.

At the V/F end it should be noted that the reduction of the supply voltage to the V/F also reduces the input range, by about 0.7V. This will reduce the input range to about 0.3V (max) for a 5V supply. The quiescent power of the V/F should be minimized by operating it with an I_t of 100μA and careful controlling any additional power loading. Because of these power supply restrictions, this type of circuit is best suited for those types of sources or transducers where little or no additional power support is needed.



a. Simple Phantom Power Driver



b. Phantom Power Driver/Regulator

Figure 6. Phantom Power Schemes

Figure 6b solves the problem of additional power, and adds considerable flexiblity to the application at both the transmitter and receiver locations.

By inserting a regulator IC (A2) between the V/F output and the receiver input, two things are achieved. First, the supply voltage to the V/F and the surrounding circuitry is buffered and regulated to a reference quality level. This allows additional precision circuitry support to be added with relative freedom. Second, the V/F square wave output delivered to the receiver (in current form) is also regulated providing independence from power supply changes and noise pickup in the cable.

In the receiver circuit several functions are performed. DC power is coupled to the transmitter via LED_1 (green), and low resistance choke L_1. The choke allows slowly varying or static DC curents to pass without developing any sizeable terminal voltage.

On the other hand, the faster edges corresponding to the V/F square wave develop a pulsed waveform across L_1, which is passed to the comparator A3. This stage re-constitutes the original square wave at the output with 15V levels.

The circuit as shown is suitable for operation up to 10kHz, and will operate at least three decades lower. In this example, the 5V reference output is divided down to 0.5V and applied to a 10k linear potentiometric transducer. The variable output of this pot is the V/F input, and FS calibration is done by trimming the terminal voltage via R2.

Load resistor R_L sets the output current level of the V/F to a nominal 2.5mA. If the supply voltage of the V/F should be changed, the resistor should be adjusted to maintain this same current. This point suggests the versatility of the circuit, as the AD584 reference IC can be programmed for either 5V or 10V. It could also be set for 2.5V, but this will not be useful to the AD654 (nevertheless, this tap is still available at pin 3, and can be used for bias or multiple reference uses). For any given output voltage programmed into A2, about 3V of headroom should be maintained for proper regulation.

A very wide range of other circuits can be driven from A2's output, particularly if a buffer output option is used. The output will be 5V ±15mV, at a TC of 30ppm/°C or better using the AD584J. Of course the same general principle of three terminal regulation can be employed with one of the more utilitarian regulator IC's if a precise output is not required. No additional load can be allowed to pulse load A2. If this were to be permitted, the step change in output current would confuse the receiver and generate erroneous output data.

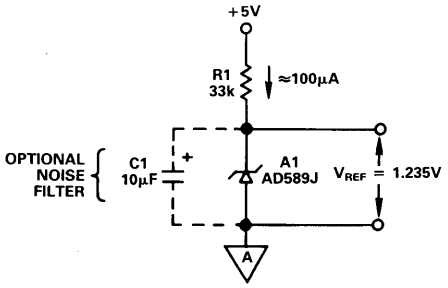
References

There are often instances where a stable reference voltage is necessary for bias, offset, or the establishment of scaling in a V/F application. Figure 7 illustrates several techniques which are useful.

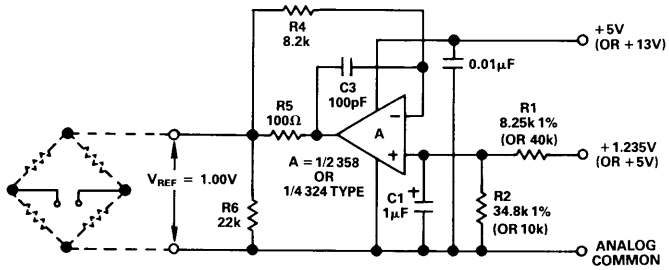
Figure 7a is a simple 1.235V reference using the AD589, a bandgap-based, low power reference diode. The low terminal voltage allows use from supplies down to 5V, therefore this type of circuit is applicable to virtually any AD654 use.

Figure 7b shows how appreciably higher source currents can be provided from a given reference source. It is applicable to either a basic 1.2V source (7a), or an optional 5V source (such as 6b). In either case, the output is 1V at a low impedance level, so several mA can be sourced for driving bridge transducers, servo pots, etc.

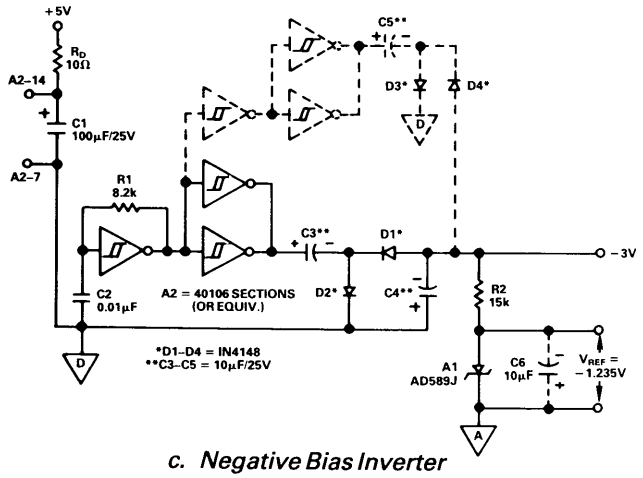
Negative bias voltage from a positive supply is a problem that can be handled with a simple dc/dc converter when the overall load power is low. An example is shown in Figure 7c.



a. Basic Positive Bias Reference Source



b. Buffered Low Power Reference



c. Negative Bias Inverter

Figure 7. Reference Circuitry

This circuit is an 8kHz inverter using CMOS inverters and an output p-p detector. With a 5V supply, it will develop a −3V output capable of 1-2mA drain. Regulation as shown is relatively poor, but can be optionally improved by using spare inverter sections to provide full wave rectification (shown dotted). If a negative reference potential is required a 1.2V reference diode can be used, as shown.

An input decoupling filter for the inverter is shown (R_D-C1), which will minimize the potential for noise to be injected back into the +5V supply.

Signal Multiplexing

When a variety of transducers are required to interface with a common data acquisition system, one solution is to use separate instrumentation amplifiers for each channel, followed by an analog multiplexer which drives a (single) V/F converter. However, in many cases a more economic solution may be realized by using a dedicated AD654 per channel and multiplexing these outputs digitally. Such a circuit is shown in Figure 8.

The open collector feature of the AD654 makes this easy to implement. In this application, all the V/F circuits operate continuously and can have a variety of input scales. For a measurement, only the V/F device having its output emitter pin grounded (2) through the "n" decoder (or other digital switching element) actually transmits an output. Note that the common V/F supply voltage must be high enough to accommodate the highest individual positive input voltage. V_{CC} can be any appropriate logic level, and can be different from $+V_S$, if necessary.

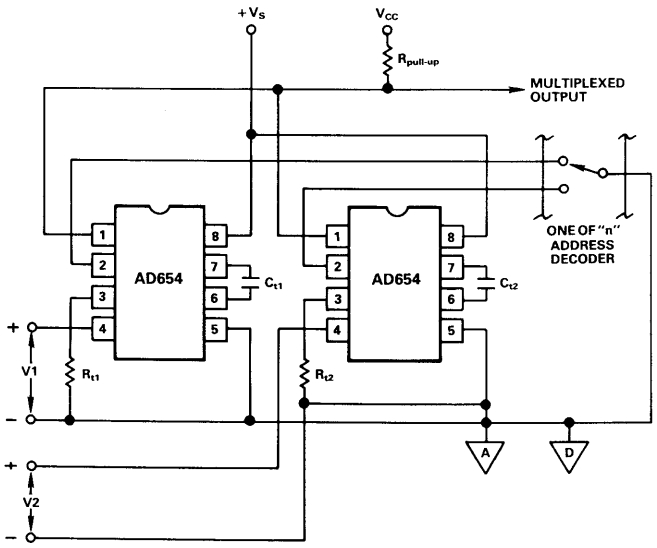


Figure 8. Signal Multiplexing

Transformer Coupling

Coupling a V/F output signal between two isolated logic grounds via a pulse transformer can be both economical as well as useful for frequencies up to about 10kHz. An example of a 1V/10kHz transformer coupled V/F is shown in Figure 9.

In this circuit the AD654 is operated at an I_t of 100μA in order to minimize power consumption, a factor important for many isolated power hookups. T1 is a miniature,

printed circuit mount telecommunications type 1:1 isolation transformer operated in a pulsed mode.

The V/F produces an output square wave, which is shaped into negative going pulses by the low power CMOS logic for each transition. The pulses are easily transmitted across the transformer's isolation barrier, even at the extremely low frequencies which are well outside the transformer's normal bandwidth.

At the secondary side, bias is applied to one end of the transformer and coupled to a CMOS Schmitt type inverter. The hysteresis of this stage provides noise immunity as well as the necessary latching function to transform the alternate (+) and (−) pulses back into a square wave.

The supply voltage shown for the AD654 is +9V and is an example of a low power circuit compatible with a simple isolated dc/dc converter or a low cost battery. Other supply voltages, consistent with the CMOS logic, can be used if the drive to T1 is maintained at a high level.

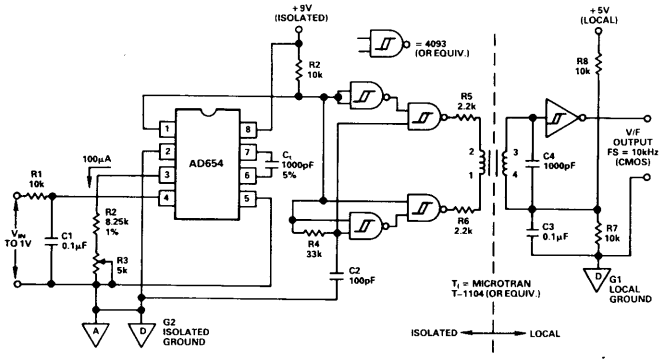


Figure 9. Transformer Signal Isolation

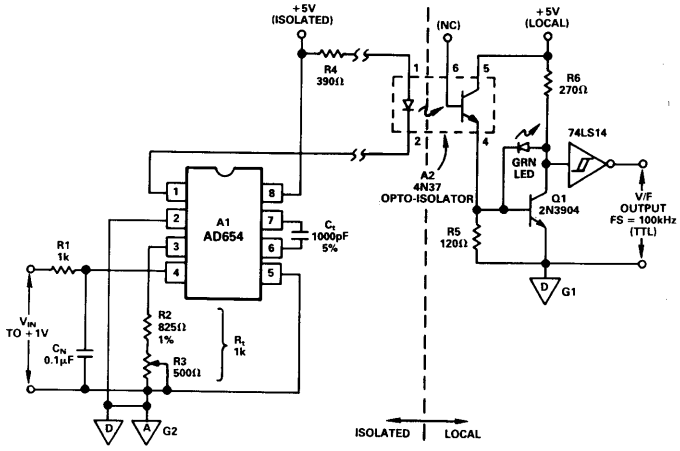
Optoisolator Coupling

A very popular method of isolated signal coupling is via optoelectronic isolators, commonly called optoisolators or optocouplers. In this type of device, the signal is coupled from an input LED to an output photo-transistor or photo-diode, with light as the connecting medium. This technique allows DC to be transmitted, and is extremely useful in overcoming ground loop problems between equipment. It is also applicable over a wide range of speeds and power. In fact, a very large percentage of V/F applications can potentially be useful with opto or other types of isolated coupling, so a number of useful circuit examples are given.

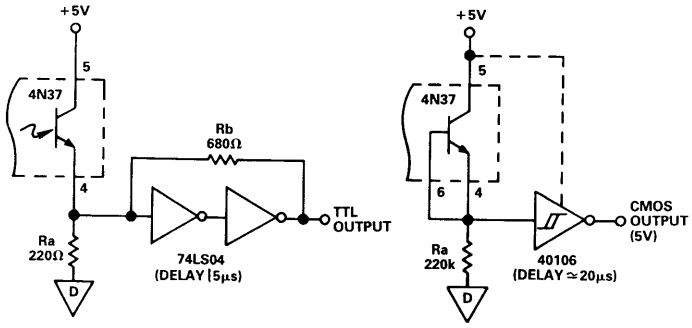
General Purpose, Medium Speed

General purpose versions of optocouplers abound, using infrared LED's for input and photo-transistors for output. This type is very cost-effective for general purpose work and can be useful up to about 100-200kHz with proper interfaces. Higher speed devices are also available for applications up to as high as 1MHz or more. The tradeoff between the two classes is generally cost, which is relatively high for the higher speed units.

Figure 10a shows a general purpose isolated V/F circuit using a 4N37 opto-isolator. A +5V power supply is assumed for both the isolated (+5V ISOLATED) and local

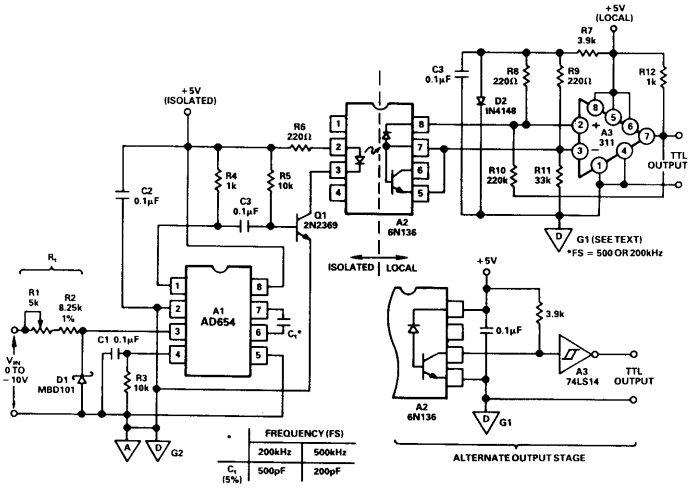


a. Medium Speed, General Purpose (100kHz)



a1. TTL Output Buffer

a2. CMOS Output Buffer (Diode Mode)



b. High-Speed Isolated V/F

Figure 10. Opto-Coupler Isolation

(+5V LOCAL) supplies. The input LED of the isolator is driven from the collector output of the AD654, with a 9mA current level established by R4 for high speed as well as for a 100% current transfer ratio (CTR).

At the receiver side, the output transistor is operated in the photo-transistor mode; that is, with the base lead (pin 6) open. This allows the highest possible output current. However, for reasonable speed in this mode it is imperative that the load impedance be as low as possible. A single transistor stage current-to-voltage converter does this, providing a dynamic load impedance of less than

10Ω and interfaces with TTL at the output. Q1 is this stage and achieves 2μs (typical) delay times for both the ON and OFF transitions. This allows the stage to be useful to as high as 100kHz. The circuit values around the V/F are for 100kHz, but other input configurations can be used.

In the circuit of Figure 10a, the values around the 4N37 are optimized for speed at the expense of power. If simplicity or lower power operation is desired, alternate output side buffer-interface connections can be used. For a simple (albeit slower) TTL buffer the hookup of Figure 10a1 can be used. If low power is key, Figure 10a2 is suitable. Both stages provide TTL or CMOS 5V output levels, and should use Schmitt type amplifiers for the fastest output transitions and the nonambiguous switching of downstream logic stages.

High Speed

For isolated V/F uses appreciably above 100kHz, an optocoupler specified for high speed is the best choice. This can be achieved several ways, including user-designed high-speed photo-diode type isolators with high-speed output buffers, or complete integral-buffer high-speed TTL output optoisolators such as the 6N137 types. Of these two, the former is illustrated below.

Figure 10b shows how an isolated photo-diode V/F output coupler suitable for a FS frequency of up to 1MHz can be implemented. In this circuit, a high-speed, separate photo-diode/transistor optoisolator is used (the 6N136). For this particular use, the 6N136's internal transistor buffer is not used, but the high-speed diode between pins 7-8 is applied to take advantage of the low inherent delays.

The V/F portion to the left is a −10V, 200 or 500kHz FS circuit using the AD654 from an isolated +5V supply with a 16mA output drive. Other input arrangements can also be used, however the input mode used here allows the maximum V/F linearity to be achieved. The AD654's I_t should be set at no lower than 1mA for best speed and the Q1 output driver stage for the LED is recommended. The V/F can be easily set up for either 200 or 500kHz FS operation as shown in the table. The best overall linearity will be attained at a 200kHz FS and it can be lower than 0.1%.

At the receiver, resistors R8-R9 act as a differential, low impedance load resistance for the photo-diode which is operated in a photo-voltaic mode. A3, a standard 311 type comparator, regenerates the logic state of the diode, producing 5V TTL levels at its output. The stage has ON and OFF delays of about 200ns (or less). Thus, it is useful at speeds up to 1MHz or higher, depending upon the comparator used. The 311 is the upper speed limit to this coupler. However, even the general purpose 311 is capable of tracking the AD654 speed at 500kHz and its single 5V supply operation is attractive for reasons of simplicity.

Note that the 6N136 coupler also allows the more conventional use by applying the photo-diode output current to the built-in NPN transistor as a saturated logic stage. This mode, which is an alternate option for this circuit, is shown in detail in the inset. It is attractive for intermediate speeds, delays on the order of 1μs or less, since it does not require the comparator stage used here. Note that a Schmitt type TTL buffer is still recommended.

Single-Supply Bipolar V/F

In many applications using the AD654, a +5V power supply may be the only power supply available. This makes it a challenge to process bipolar signal inputs without generating additional supply voltage(s). Figure 11 illustrates a novel circuit which can in fact processes inputs of ±10V, with a +5V supply on the AD654.

The bipolar input capability is achieved by A2-a, a precision rectifier stage which scales a 10V input to +1V across R3. A2-b detects the SIGN of the input and is HIGH for positive inputs. The 1V scaled output from A2a is always positive and is fed to the AD654 (+) input, with optional noise filtering by C3.

The V/F is scaled for a 10kHz FS frequency with a 10V input. If desired, compensation for rollover error (gain difference between equal magnitude positive and negative inputs) can be added by trimming R3 for a positive gain equal to the negative gain. R12 sets overall scale factor (adjusted for 10kHz with −10V input).

The SIGN output is handled in a novel manner, allowing both frequency and SIGN to be transmitted on the same serial cable. The output from the AD654 is steered by gates A3-b and A3-c, which are controlled by the sign bit. For a given sign, one of the one shots will be triggered and combined by gate A3-d. The resulting output pulse train follows the input frequency, but with a pulse *width* encoded for the sign. A width of 38μs corresponds to a negative input sign, while 65μs indicates a positive input.

At the decoder, the logic simply clocks a D flop 50μs after the leading edge, decoding a one for a positive sign, and lighting the indicator.

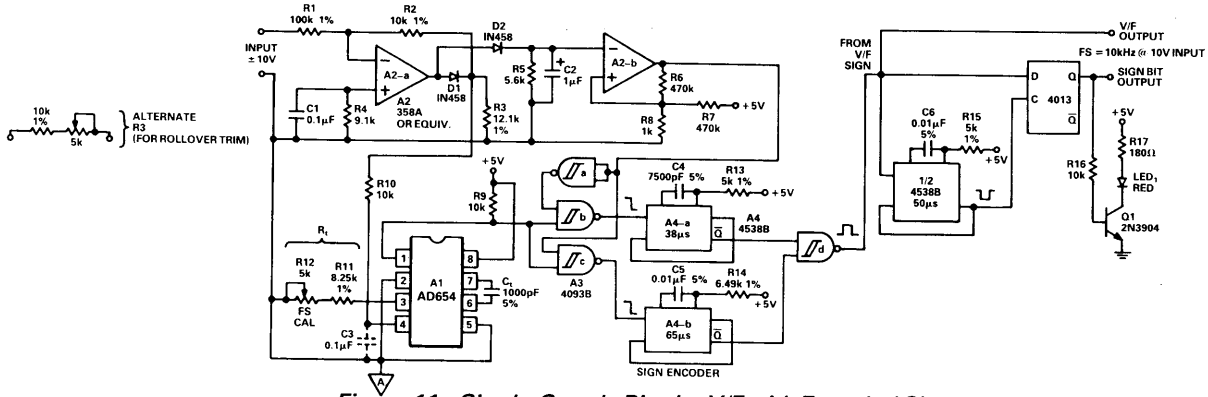


Figure 11. Single-Supply Bipolar V/F with Encoded Sign

Offset Scaled V/F

Figure 12 illustrates a method of offset scale operation with a bipolar input signal. By the very nature of this application bipolar supplies are assumed; in this case they are ±5V.

This circuit is designed for a basic range of ±0.5V, as seen at the AD654's (+) input. This is raised to ±1V by the input divider, allowing trim of span or alternate input scaling (shown here as a 10V option).

The basic frequency for zero input is defined by the quiescent offset current, which is derived from a negative reference of 1.235V, A2. Since the timing resistance will drop 1.235V for a zero voltage input, 1.235V becomes the effective V_{IN} for the calculation of center frequency. C_t is chosen in a conventional manner. Note that for best stability an NPO type should be used. While the linearity will not be as low as that of polystyrene, little difference will be seen in this application, since the oscillator always sees a relatively narrow frequency range.

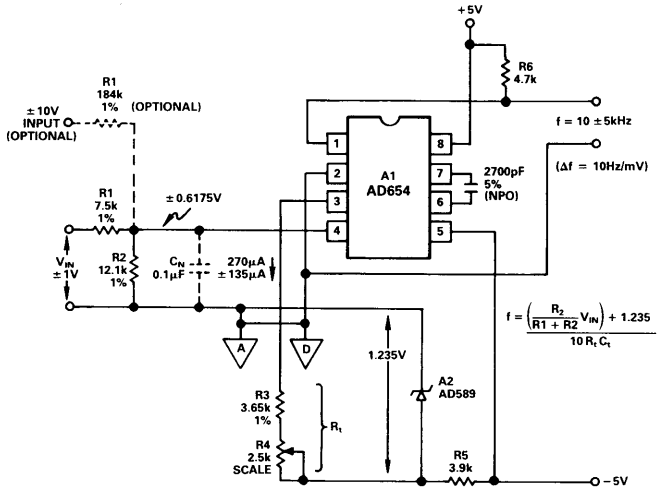


Figure 12. Offset Operation, ±1V (or ±10V) FS

In this example, 10kHz is the center frequency and a ±1V input swings the frequency ±5kHz (15kHz to 5kHz). The frequency swing sensitivity is set by the R1/R2 ratio which scales the AD654 input to ±0.6175V. This in turn changes the current in R_t ±135μA for ±5kHz.

An offset scaled V/F such as this is a convenient method of transmitting ac or bipolar data without the complication of sign bits and zero crossing detectors. The data can be recovered at the receiver site via an F/V converter and ac coupling (see Figure 20), or via an FM discriminator system.

Thermocouple Source Temperature-To-Frequency

Figure 13 illustrates another method of offset scale operation, one very much related to the more general scheme of Figure 12. In this case, the signal source to the V/F is the AD594 (AD595) thermocouple signal conditioner, allowing measurement of temperatures with either a type J or type K thermocouple. In this application bipolar supplies are again assumed to be ±5V.

This circuit is designed for a basic range of ±1.0V, as seen at the AD654's (+) input. This signal is produced by A2, which is either an AD594 (type J) or an AD595 (type K), and corresponds to a signal output of ±1V for a basic ±100°C span. The AD594(5) part of the circuit consists only of A2 and the thermocouple ground return resistor, R3. All the amplification and offset necessary is within A2, which operates from ±5V supplies. The A2 output signal is fed directly to the AD654 through a low pass filter, R1-C1.

The basic frequency for a zero °C input is defined by the AD654 quiescent timing offset current, which is derived from a negative reference of 1.235V, A3. The timing resistance will drop 1.235V for a zero voltage V/F input and this part of the circuit is otherwise similar to Figure 12. With the values shown for R2 and C_t, the output frequency becomes 4574Hz, at 0°C.

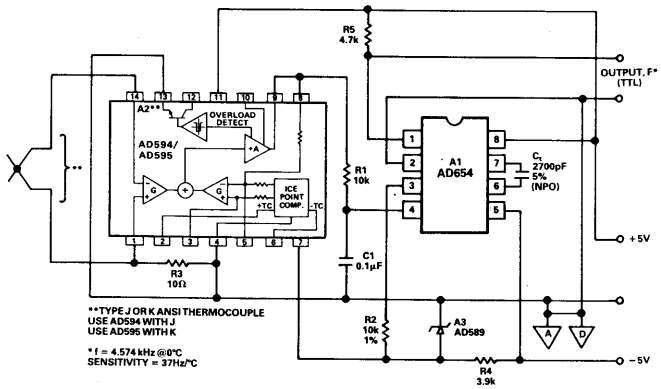


Figure 13. Thermocouple Source Offset V/F

As can be noted, this circuit has no calibration provision. It is intended to be used with an F/V converter in order to trim the output voltages for zero and full scale temperatures. Used with the AD650 or a similar F/V and followed by a differential amp to shift zero scale to zero volts dc, trim can be easily accomplished. The F/V's full scale calibration is used for the high-temperature calibration point and the differential amplifier offset for zero (at 0°C, or freezing).

Resistive Transducer Interfaces

With the wide dynamic range of control inherent to the AD654, it functions very well as an A/D conversion device to read out linear resistive transducers, such as servopots, etc. A basic scheme to accomplish this is shown in Figure 14.

This circuit simply applies a stable dc reference voltage on the order of +1V across the pot. With a stable excitation on the pot, the output voltage will represent the product of the fractional rotation α and V_{REF}. Since V_{REF} is unity, the output frequency is, therefore, directly proportional to α, as shown by the expression.

The major V/F conversion error of this circuit will likely be that of the AD654's basic nonlinearity, which can be 0.1% (or better). With a 50k pot, the worst case bias current induced error will be seen at mid scale, but this still will be

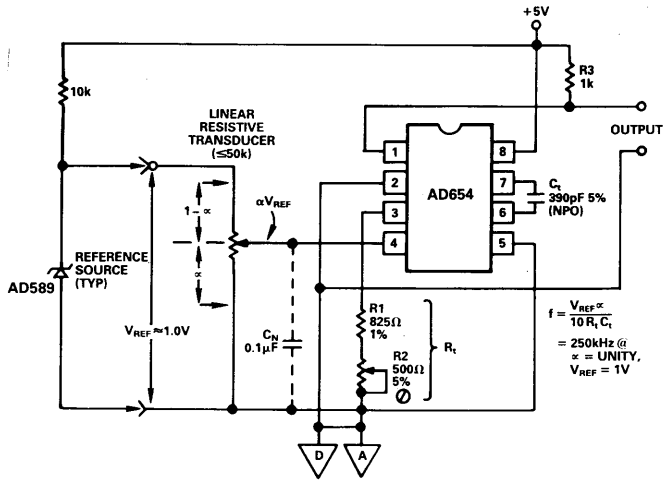


Figure 14. Resistive Transducer Interfacing

typically under 1mV. With the values as shown, the full scale frequency is 250kHz when α is unity.

To implement this type of circuit, virtually any stable 1V reference source can be used but the output impedance should be low. This is important, to minimize the possible variations of the reference source with variable pot loading. A buffered reference (such as Figure 7b) is therefore suggested. Reference voltages *higher* than 1V can be used if the AD654 is powered from a higher supply voltage. For frequencies above 200kHz, output buffering may be used (Figure 5b).

Photosensitive Transducer V/F's

Photosensitive sources such as phototransistors and photodiodes are easily interfaced to the AD654. An example of a phototransistor source is shown in Figure 15. This figure illustrates how a phototransistor can be biased at a defined collector-emitter voltage by the AD654, and the resulting current output converted to a linearly proportional frequency. For a sensor photocurrent of Iλ, this current becomes equivalent to I_t in the frequency expression, as shown.

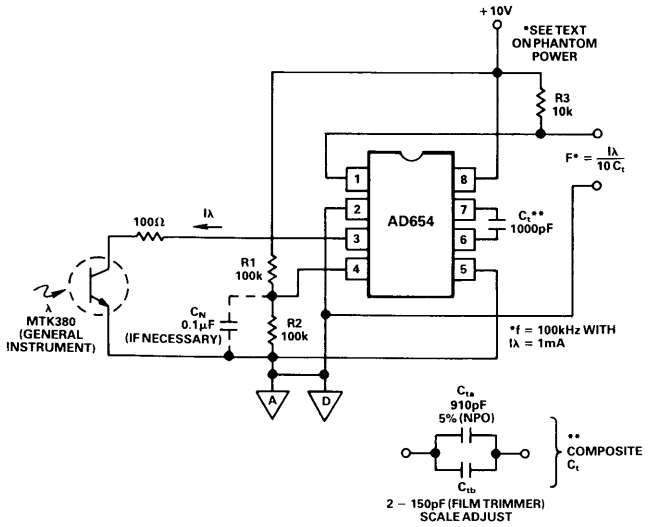


Figure 15. Phototransistor Photosensitive Sources

Since the AD654's internal op amp will bias pin 3 to the potential applied to pin 4, the voltage divider R1-R2 and the supply voltage will determine the effective C-E potential. Here this voltage is 5V, but it could be any voltage within the common-mode limits of the AD654. With a general purpose sensor such as the MTK380, operation is specified at a 1mA current with a 5V bias. An important point for this circuit is that it can easily accommodate any sensor. The divider can be bypassed for noise if necessary and, if maximum bias voltage stability is required, R2 can be made a zener or stable reference diode.

For an output photocurrent of 1mA, this circuit as shown will produce a frequency of 100kHz with a C_t of 1000pF. Calibration can be a problem since not all sensors and/or sources will be controlled as to scaling. The variable C_t shown in the inset will allow for about a 10% scale variance but even this may not be enough. If the sensor and V/F are remote, hardware calibration may not be feasible at all. For either case, scale calibration for a specific light input can be accomplished via software. Note that the circuit can be phantom powered easily, since the transducer is biased completely by the V/F.

Photodiode Sources

Interfacing a photodiode to the AD654 V/F is simple and can be accomplished two ways. The first is the photodiode can be biased to a fixed terminal voltage simply by substituting it for the phototransistor shown in Figure 15. Similar comments apply as to calibration, terminal voltages, etc.

The second is the photodiode can be operated in its photo-voltaic mode, with a basic terminal voltage of zero and a minimum load impedance. A circuit which accomplishes this is shown in Figure 16.

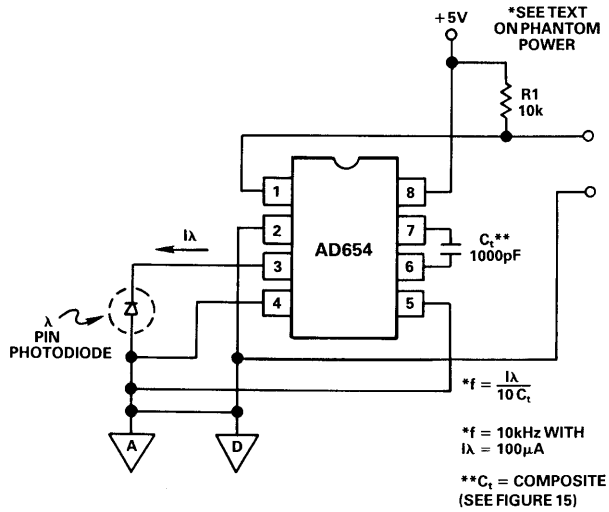


Figure 16. Photodiode Photosensitive Sources

The simplicity of this circuit is appealing, since the diode is merely tied between the two op amp inputs with the (+) input grounded. C_t is selected for the desired frequency and is the only circuit part critical to operation. Calibration in general has the same set of considerations as does the phototransistor, with similar solutions. It can be done by

making a small part of C_t a trimmer (as shown in Figure 15), or via software. Like Figure 15, this circuit is also easily used with phantom powering.

A legion of photo devices are available which are potentially suitable for use in either of these two circuits, operated over the wide range of currents/frequencies accommodated by the AD654.

Temperature-To-Frequency Converters

Low cost IC temperature transducers are both cost effective as well as easy to apply to remote measurements. Two cases are shown in Figure 17.

In Figure 17a, an AD592 IC temperature transducer is interfaced to the AD654 in a manner similar to that of the phototransistor (Figure 15). In the case of the AD592 the minimum bias voltage is 5V, so the circuit as shown will work down to 10V supplies (it will also work with higher supplies).

The AD592 produces a 1μA/K current output which drives pin 3 of the AD654. With the timing capacitor fixed at a value of 0.01μF this produces a frequency which is scaled as 10Hz/K; that is, 298K = 2980Hz. Since temperature is the parameter of interest, a 0.01μF NPO ceramic capacitor is used for lowest V/F TC. Calibration of this circuit can be accomplished either by using an input current divider or simply by subjecting the transducer to an ice reference and measuring the output frequency. If it differs from 2730Hz, software scale corrections can be applied to the measurement. A hardware calibration can be achieved by scaling the output a decade higher using a variable C_t of 1000pF.

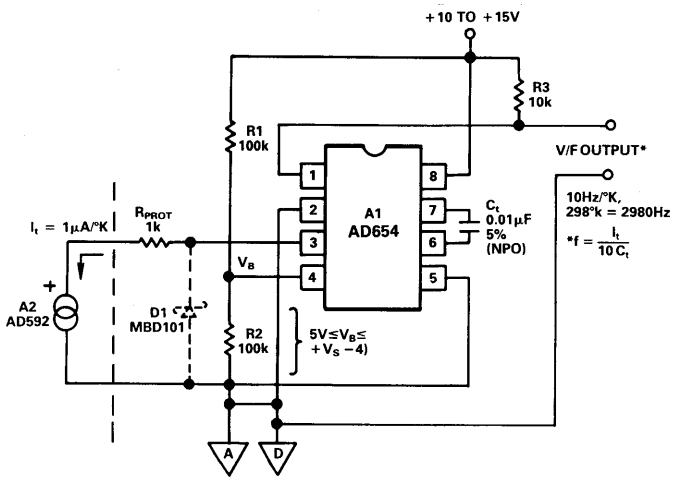
Like the photosensitive circuits, this circuit is a good candidate for phantom powering. Optional components include protection resistance R_{PROT} and D1 (which are only necessary if it is possible for A2 to contact dangerous external voltages).

Figure 17b shows how the same basic transducer can also be used with a current offset to produce a Centigrade scaled V/F.

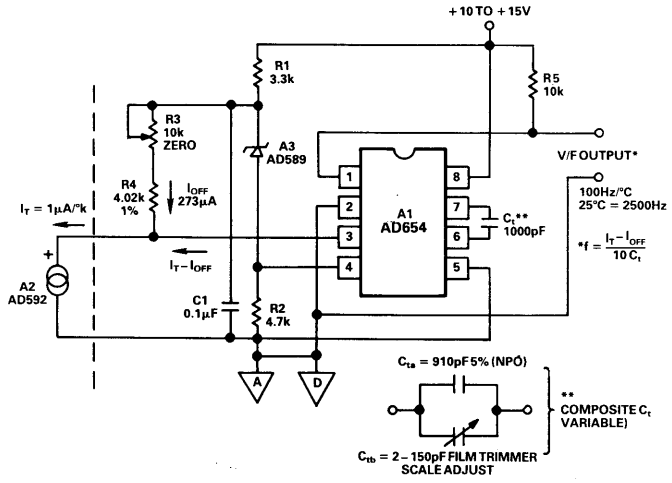
In this circuit, the AD592 drives the AD654 in the current input mode. The output of the AD592 is I_T and is scaled at 1μA/K. However, in this case a fixed offset current I_{OFF} is subtracted from I_T. Thus, what the V/F actually receives is the input $I_T - I_{OFF}$.

The V/F current input is offset by 273μA as established by R3-R4 and corresponds to 273K, or 0°C. Thus, this point is the zero frequency scale of the V/F. Above 0°C (273K) the V/F operates with a sensitivity of 100Hz/°C. An interesting feature of this particular circuit is that the offset current is regulated by the "floating" reference diode A3, even though the common-mode input to the AD654 can vary with supply voltage.

Trimming the circuit for zero scale calibration can be accomplished by placing sensor A2 in an ice bath reference and adjusting R3 (ZERO) until the output frequency just stops. To complete the calibration, the circuit is adjusted for 10,000Hz with A2 at 100°C (boiling water). This



a. Kelvin-Scaled Temperature – to – F



b. Centigrade-Scaled Temperature – to – F

Figure 17. Temperature-Frequency Circuits

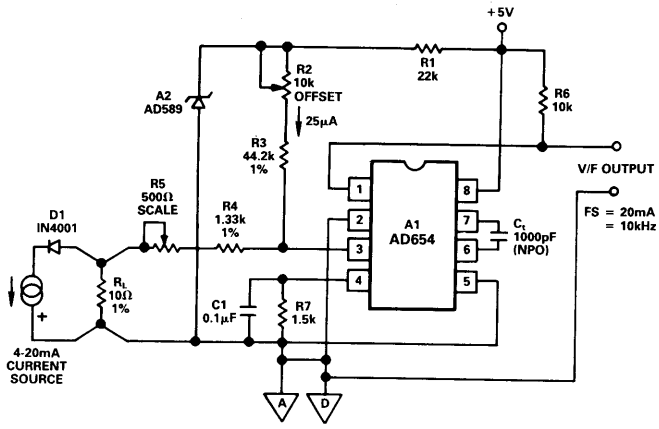
is done simply with a hardware trim via C_t with the film trimmer. Here, the trimmer is C_{tb} (SCALE) while the bulk of the timing capacitance (C_{ta}) is an NPO type. Note that the trim is best done with a plastic tuning wand since C_t is floating. As Teflon and polypropylene film trimmers are available up to about 200pF, this type of tuning can be effective for circuits using a C_t of 1000-2000pF. The scale trim should be repeated once for best accuracy.

4-20mA Current Loop Conversion Circuits

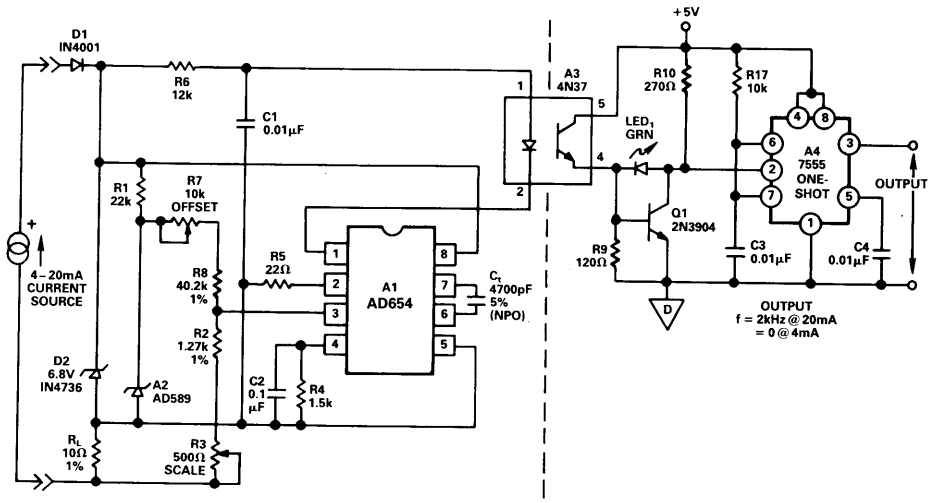
The 4-20mA industrial current loop is a commonly used interface. Converting such input signals into a proportional frequency is relatively easy and allows ac transmission techniques to be used. Two examples are shown in Figure 18.

The most straightforward way to convert a 4-20mA signal is to convert the current to a voltage with a precision load resistor, then convert the voltage to a frequency with a V/F, and then transmit the signal in frequency form to a microprocessor for removal of the offset (i.e., the frequency corresponding to 4mA).

The offset in *current* form can also be removed at the V/F stage as shown in Figure 18a. Here, the load R_L converts the 4-20mA signal to a 40-to-200mV voltage which drives the V/F.



a. Offset Conversion of 4 – 20mA Signal



b. 4 – 20mA Loop Powered, Isolated to F

Figure 18. 4 – 20mA Conversion Circuits

The bias network R2 through R5 provides an input voltage offset of 40mV so that the 4mA zero scale will produce a zero output frequency. The basic V/F scale factor is set via R4 + R5. From 40mV to 200mV across R_L the AD654 sees a 160mV change, thus R_t needs to be about 1600Ω for an I_t of 100μA. With a FS I_t of 100μA, C_t is 1000pF for a 10kHz FS frequency.

Calibration is achieved by applying a 20mA input and trimming R5 for 10kHz out. Then, with 4mA applied the output can be checked for zero frequency, and trimmed (if necessary) with R2. Note that the two adjustments (R5 and R2) are interactive. Because of this factor, the calibration process should be repeated at least once. The circuit as shown assumes a floating source, so D1 might be necessary for reverse protection. It can be eliminated for a known input polarity but even if included it will not harm accuracy. Since the R_L terminal sense voltage is very low with this circuit (200mV) line voltage drops are not likely to be a problem.

The circuit of Figure 18b is an interesting variation of the basic one in Figure 18a as it is powered by the *loop current*. This is possible since the lowest loop current of 4mA is higher than that required to bias the AD654 plus the support circuitry. The advantage of this technique lies not just in the fact that the power is "free", but that it allows a completely floating I/F converter to be implemented using isolation techniques.

In this circuit the offset and scaling of the AD654 is very close to that used in Figure 18a. D2 clamps the supply voltage of the V/F to 6.8V and the offset reference diode A2 is biased from this voltage by R1. The AD654 V/F sees virtually a constant supply voltage for loop currents above about 2mA.

Since the desired LED drive current of ≈10mA is greater than the low scale input current an alternate technique must be used; in the case here this is a shift of duty factor for the LED drive. Thus, getting the signal out of the V/F and into logic stages requires a pulse forming network R6-C1. This allows the charge on C1 to be dumped in the opto isolator's LED once per cycle of oscillation, which in turn is coupled thru to Q1 and regenerated by the one shot A4. The technique works over the entire 4-20mA range, with the peak discharge current safely limited by the AD654's output transistors.

This circuit is scaled for a 2kHz FS frequency with a 20mA FS input current. The recharging considerations of C1 prevent it from working at appreciably higher frequencies. While this low frequency would appear to suggest the use of a low-speed optoisolator and buffer, such is not the case. The discharge of C1 is fast; on the order of a few microseconds. This requires the relatively fast buffer, Q1. The use of the following one shot is optional; as shown it produces positive 110μs pulses.

This circuit is quite valuable wherever current source signals of 4mA and up are used and isolation is required, whether or not the offset bias function is used.

Digitally-Tuned Switched Capacitor Filter

Switched capacitor (switchcap) filters using IC packaged state variable building blocks have become quite popular. Two reasons for this fact are the all-around utility of the state variable filter itself, which allows all standard filter modes to be resistor and/or pin programmed, and the ability to easily and precisely tune the filter center frequency via a clock input. A variable rate clock such as the output of a V/F can readily drive a switchcap filter effectively, avoiding cumbersome ganged pots and limited range tuning. This is particularly important when filter sections are cascaded.

Figure 19 is an example of a 12-bit binary, digitally tuned switchcap filter using the MF10C CMOS filter building block driven by an AD654. In this circuit, the AD654 V/F is operated as a single supply digitally programmed clock source. With the V/F device operated from a +10V supply the output will be a 10V square wave (f_{CLK}), which satisfies the clocking requirements of the MF10C filter.

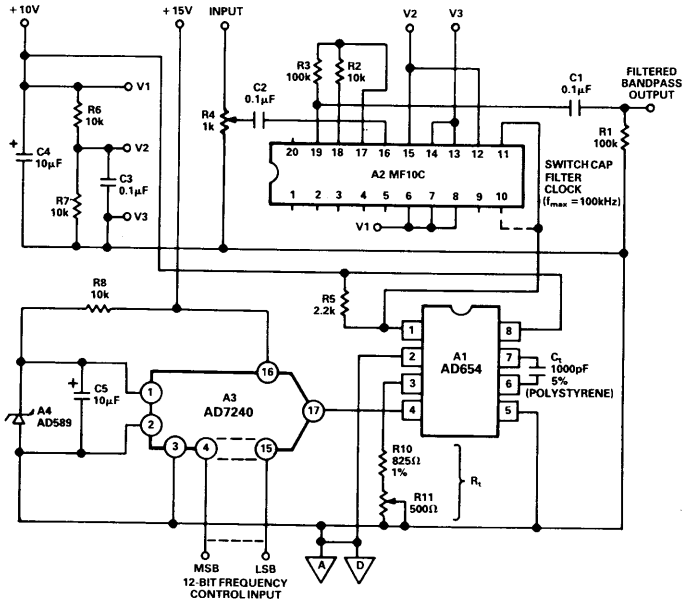


Figure 19. Digitally-Tuned Switched Cap Filter

A2 and the associated components comprise the V/F tuned switchcap filter. As connected here, the MF10C is operated in its "1a" bandpass mode with a gain and Q as determined by R3/R2. The signal to be filtered is applied across input level control R4 and fed via C2 to the filter. The filtered output appears at pin 19 and is ac coupled to the output by C1. Note that the MF10C is comprised of *two* filter sections; only one of which is operated in this hookup. It is also capable of operating in the HP, LP, AP, and notch modes (see manufacturer's literature).

As operated here the filter center frequency is $f_{CLK}/100$, where f_{CLK} is the V/F frequency. This in turn is programmed by the AD7240 D/A with 12-bit control resolution. Thus the filter's center frequency is programmable over a dynamic range of 2^{12}. The precision of tuning will be as good as the f_{CLK}/f_O spec of the MF10C, which is ±1.5% or better. This assumes calibration for an actual filter frequency of 1kHz with an all 1's D/A input. Further discussion of this D/A tuning technique of the AD654 is covered in a later application (Figure 23).

This versatile circuit cannot only achieve all the filtering functions noted above, but it can also be used with the AD654 in any of the standard V/F input control modes, tuned either electronically or manually. A simple, manually variable clock generator (Figure 22 series) will allow tuning of filtering functions over a wide range.

Wide Range Precision PLL F/V Converter

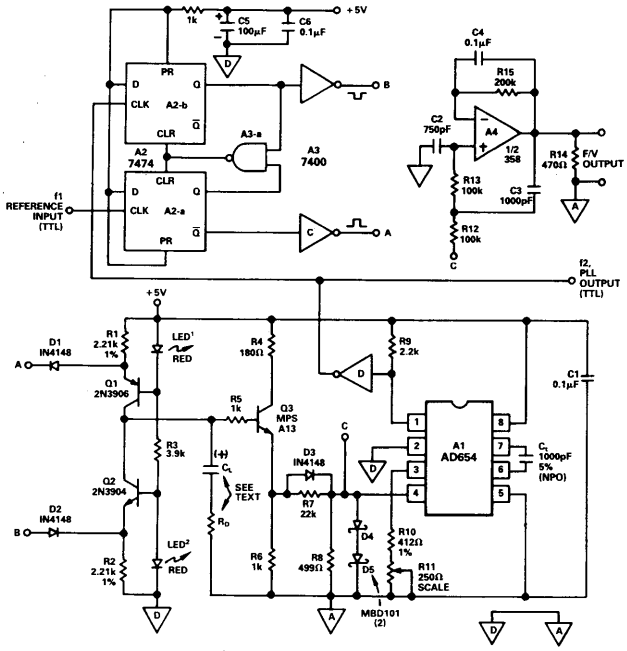
The phase locked loop (PLL) has become a familiar circuit building block, one routinely used for a variety of signal processing tasks. Since a number of readily available, standard, dedicated chips perform the PLL function, a logical question would be why one would need to use a V/F. The answer to this is two-fold:

1) To achieve a greater dynamic range of frequency lock, i.e., more than a single decade.

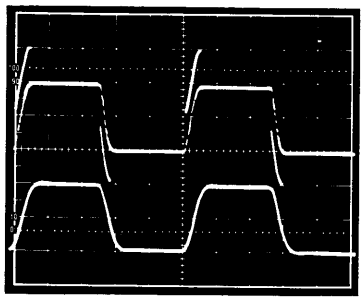
2) To implement precision F/V circuits. These performance attributes are not available from the dedicated PLL chips, but can be provided by V/F circuits.

The V/F based PLL circuit of Figure 20 uses a wide dynamic range digital frequency/phase detector as the PLL comparator. With this type of circuit the input signal can range over a very wide span and the locking characteristic is not harmonically sensitive. It accepts a TTL compatible square or pulse input, f1. As shown here, f1 can be as high as 100kHz with overranging to 150kHz. The PLL produces a square wave TTL output, f2, at the same nominal frequency as the input. This output is locked to the input in terms of both frequency and phase and is referenced to the positive going edge of f1. In addition, the circuit also produces a low-pass filtered F/V output from stage A4. This signal, a smoothed version of the V/F's control voltage, is precisely proportional to the input voltage. It can be used as a precision F/V output voltage signal or as part of a larger overall loop . . . for example to characterize specific V/F devices at test. The entire PLL circuit operates from a single +5V supply.

The digital frequency/phase detector is made up of the 7474 dual TTL D flop (A2) and the associated gate sections (A3). When the loop is in lock, a positive leading edge at f1 and at f2 clocks to a "1" at the A2-a and A2-b Q outputs, respectively. Gate A3-a resets both flip-flop sections after about 50ns. The $\overline{Q}$ and Q outputs of A2-a and A2-b are, therefore, narrow pulses coincident in time, but opposite



a. Circuit Diagram



b. AD654 PLL Performance (Fast Response Mode)
Upper Trace: Phase Detector Output (Point "C")
Lower Trace: F/V Filtered Output

Scales: 0.2V/div, 500µs/div
Source: 50/100kHz FSK @ 400Hz Rate
Condition: C_L = 0.1µF, R_d = 500Ω

Figure 20. PLL

in phase. These outputs will only be 50ns in width for the locked condition. They are buffered and used to control the sampling gate at points A and B.

The sampling gate used consists of the current source transistors Q1 and Q2, which are in turn controlled by diodes D1 and D2. For the locked condition the coincident, equal width pulses will turn on the current sources for equal lengths of time, thus no net current will flow into the loop storage capacitor, C_L. However, if Q1 is on longer than Q2, C_L is charged towards +5V; conversely if Q2 is on longer, C_L is discharged towards ground. The voltage which is stored on C_L represents the raw dc error voltage of the loop and ultimately controls the V/F. This voltage is buffered by Q3 and is fed to the V/F through the network R7-R8-D3. The Schottky diodes D4-D5 simply provide an overvoltage input clamp for the V/F to prevent a potential latchup caused by excessive dc input.

The AD654 is set up here as a 100kHz, 0.5V FS single supply V/F with a TTL output buffer A3-d. Calibration for exactly 0.5V at the V/F input at FS is achieved by R11, the SCALE control. This is appropriate for the circuit's use as an F/V, with the A4 two pole low-pass filter stage included. If the F/V output is not required A4 and the associated components are deleted, and R10-R11 can become a single 499Ω, 1% film unit.

The actual loop time constants of any PLL should be optimized towards the final intended use. In this case, the loop can be adjusted for either quick response (with modest dynamic range), or for a wider dynamic range (with slower response). For fast response, the C_L-R_D series combination is 0.1µF and 510Ω. For a wider dynamic range, they become 1µF and 160Ω. In general, faster response will be desirable for such uses as FSK demodulation, etc. On the other hand, a precision PLL F/V would likely use the greatest dynamic range option. It is, of course, possible to switch the filter time constants to allow fast lockup for fast changes, and wide dynamic range once the input frequency is stabilized.

The general method of selecting the loop components is to select C_L consistent with the desired dynamic range and/or speed, and then select R_D for the required damping. This can be done either from the equations below, or by scaling from the values noted above.

The conversion gain, K_d, is set by R1-R2 and is:

$$K_d = \frac{500\mu A}{2\pi} \qquad (6)$$
$$= 8 \times 10^{-5} \text{ amperes/radian}$$

The V/F conversion sensitivity, K_o, is:

$$K_o = \frac{2\pi f_{FS}}{V_{FS}} \qquad (7)$$
$$= 1.26 \times 10^6 \text{ radians/volt-sec}$$

where f_{FS} is the FS frequency and V_{FS} is the FS V/F input voltage. For the conditions shown, these are 100kHz and 0.5V, respectively.

The natural frequency of this second order loop will be ω_n, which is:

$$\omega_n = \left[\frac{(K_o)(K_d)}{C_L}\right]^{1/2} \qquad (8)$$

The damping factor ζ is:

$$\zeta = \frac{R_D[C_L K_o K_d]^{1/2}}{2} \qquad (9)$$

It will usually be desirable to make ζ about 0.8 for mimimum overshoot with a step input; the values listed assume this. Practical ranges of C_L are from just under 0.1µF up to 1µF or more; the smaller values allowing faster settling, the larger greater dynamic range. With C_L selected R_D can be calculated to provide the desired damping, as:

$$R_D = \frac{2\zeta}{[(C_L)(K_o)(K_d)]^{1/2}} \qquad (10)$$

Since for this particular circuit the product of K_o and K_d is simply 100, this can be simplified to:

$$R_D = \frac{2\zeta}{[100\, C_L]^{1/2}} \qquad (11)$$

Figure 20b is a photo illustrating the performance of the PLL used in the fast response mode (see conditions). For this test the input is a 50/100kHz FSK signal, which represents a 1/2 FS change. The two traces represent the V/F control input (upper) and the F/V output (lower). The dc baselines are offset for waveform comparison purposes. In the upper trace the loop is seen to produce the large dynamic errors characteristic of a slewing interval, but is damped and settles quickly to the final dc value in just over 200μs. The lower trace shows a similar waveform, with the fast ac components reduced by the filter. Reliable data recovery to logic levels is possible simply by voltage comparison of this waveform to a fixed dc reference which corresponds to 1/2 the p-p amplitude.

With the loop adjusted for wide dynamic range (C_L = 1μF, R_D = 160Ω), it will maintain a frequency and phase lock from 100kHz down to about 500Hz. Since it can also overrange to 150kHz, the total dynamic range is more than 200/1. With C_L = 1μF, settling is proportionally longer, about 2ms for the same 1/2 scale frequency step (50/100kHz).

An interesting feature of the circuit is that it requires very few precision components. C_t should be an NPO type for best stability and linearity, but R_t (R10-R11) is the only other precision scaling component. R1 and R2 should be stable film units as noted (since they set K_d), but this is not absolutely critical. C_L is best a polypropylene film for fast response applications, where the values are small (≃ 0.1μF). Where space is at a premium and fast settling is not critical, a high-voltage electrolytic can be used (such as 1μF/50V). R_D can be a fixed value type, and if desired it can be easily optimized for damping with the use of a dynamic display such as Figure 20b (top). Power supplies for this circuit should be well bypassed with low impedance at high frequency capacitors near the logic stages. The analog grounds (including R_D) should be returned to the V/F's common point as shown.

There are a number of possible uses for a PLL such as this. Note that f1 can be a divided crystal reference for synthesis uses. Similarly, the f2 output can be divided before the comparision to scale frequencies upward. This PLL circuit capitalizes on the virtues that a wide range V/F device brings to PLL applications circuits.

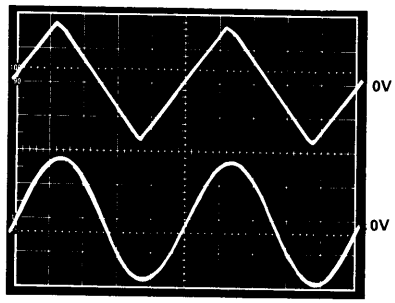
Function Generator

A general purpose function generator is a useful lab tool, as it is capable of producing the standard waveforms of sine, square, and triangle. Although the AD654 does not produce a triangle wave directly, one can be realized by differentially amplifying the capacitor waveform(s). A sine wave can be synthesized from the triangle wave. The square wave is already available from pin 1.

Figure 21 illustrates a function generator circuit based on an AD654 with a wide range, exponentially generated timing current for frequency control. This allows a standard linear pot to be used for a 4 decade control range without crowding the low end of the control span.

The control current generator is comprised of A2, A3, and Q1-Q2. This circuit produces a current from the collector of Q2 which ranges downward as controlled by the FREQUENCY control R9. R2 calibrates the high end of the scale for a 100kHz output while R6 sets the lower end to 10Hz. Q1 and Q2 are a matched pair, with high gain (2N5089, etc.).

Dual op amp A4 and single device A5 make up a low bias current, high-speed buffer for the timing capacitor. For the input stage, nothing other than a high slew rate FET input device should be used, to preserve the V/F dynamic range. The output of the instrumentation amp is from A5 and is a ground referenced, 3.6V p-p triangle wave. If the resistor ratios are matched as shown, this waveform will have a negligible dc component. R14 serves generally as an amplitude control, but is best adjusted for minimum sine wave THD (below).



Output Waveforms

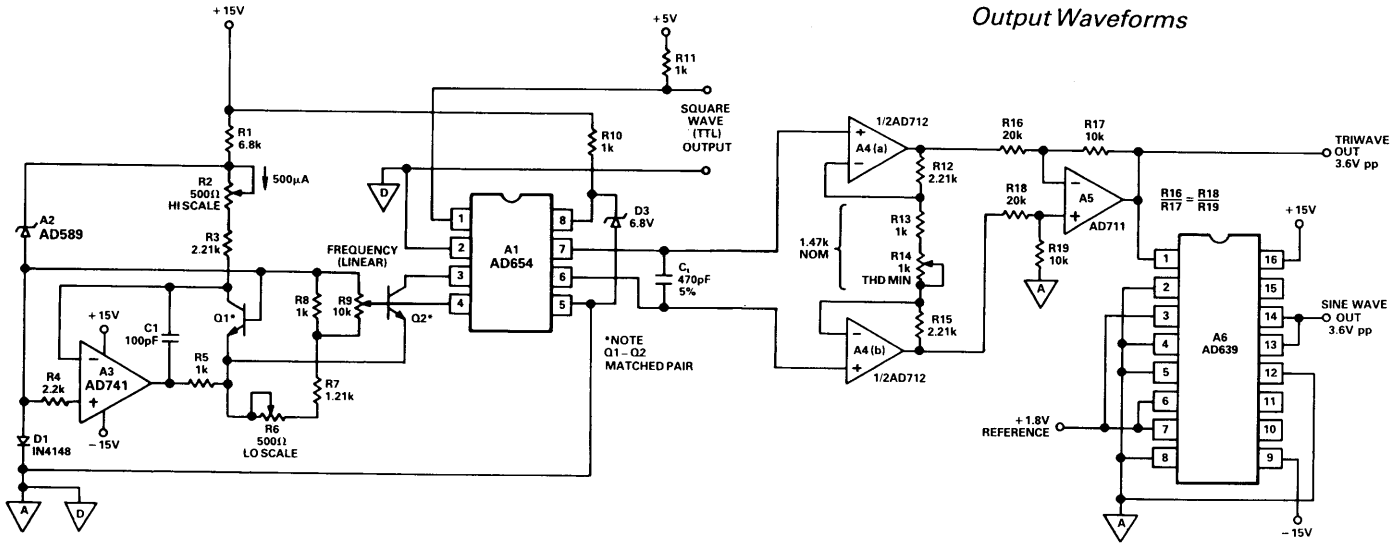
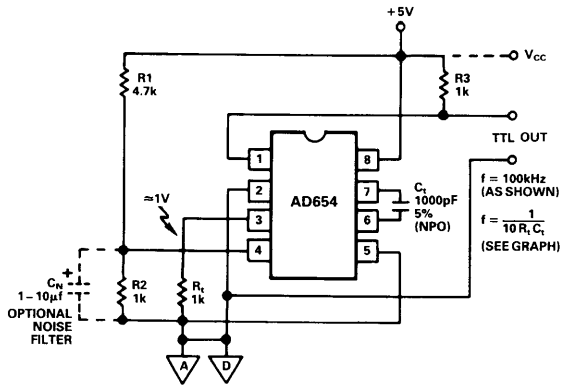


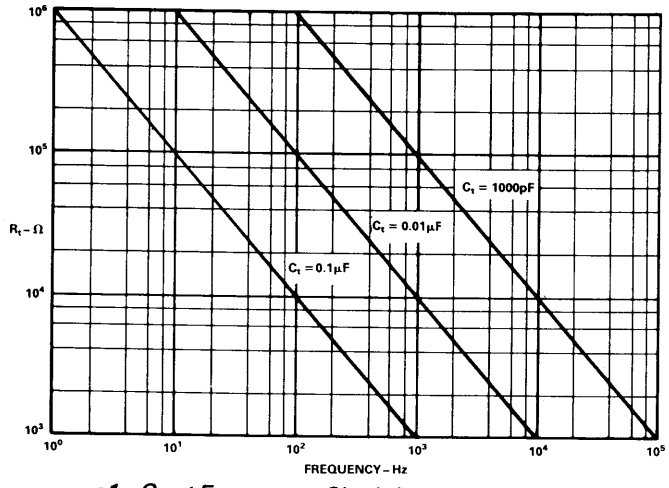
Figure 21. Function Generator

A6 is an AD639, a precision trigonometric function generator capable of (synthesized) sine wave THD as low as 0.02%, given an input triangle of sufficient linearity. With a triangle wave input amplitude of twice the device's 1.8V reference amplitude at pin 6 the chip produces a low distortion sine wave of a 3.6V p-p amplitude. Since the AD654 triangle taken differentially is 1.8V p-p, the IA net gain requirement is 2 for an optimum triangle wave drive to the AD639. The IA gain is best *trimmed* to the nominal gain of 2 via R14. This is done using the lowest observed output sine wave THD as an adjustment criterion. This allows the various circuit tolerances to be adjusted out and guarantees lowest THD. The AD654 triangle wave as it is used here is not actually good enough to take complete advantage of the AD639's low distortion capability. Nevertheless, the measured THD in this circuit is 0.5% over the full 100kHz range (after trim). Some improvement in THD performance can be expected if the AD654 is operated towards a higher I_t, such as 1-2mA. The photo indicates the quality of waveforms attainable with conditions as shown.

This circuit is useful as it is shown for general purpose work, with buffered triangle and sine wave outputs and a TTL square wave output from A1. It can easily be adapted to other means of frequency control such as the many other voltage input options throughout these notes. Also, the log control input can be enhanced further as shown below (Figure 26).



a. Simple TTL Clock Source (Fixed Frequency)



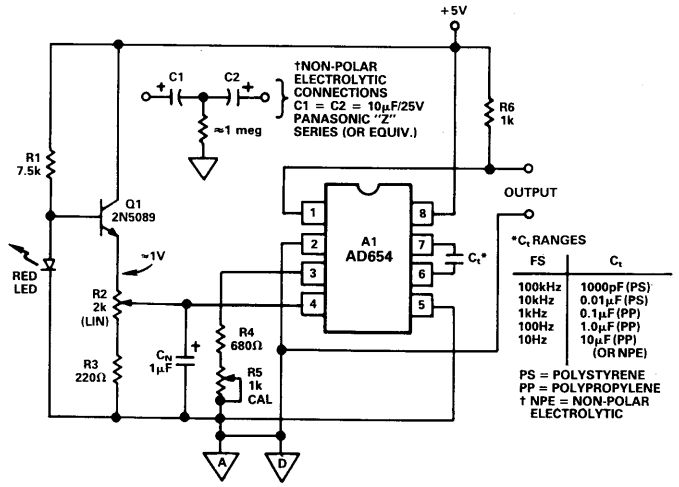
a1. Spot Frequency Clock Source Nomograph

Clock Sources

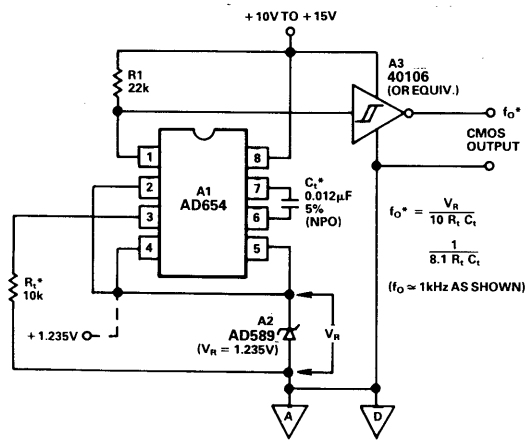
Not only is the AD654 useful as a wide range controlled frequency source, it is also useful as a stand-alone clock source. Here, the general distinction is that clock sources are not highly dynamic in terms of frequency control. Attributes of the AD654 as a fixed frequency clock source include the ease of logic output adaptation, low power, and the ease of tuning when required. Figure 22 illustrates a number of useful clock circuits.

One of the simplest clock sources possible with an AD654 is shown in Figure 22a and is suitable for TTL or CMOS uses. Note that even if the circuit is powered from +5V the output can be pulled up to *higher* voltages, such as 10 or 15V CMOS. For a control voltage, the 5V bus is simply divided down to 1V, and used as an input (with optional filtering). The output frequency is the expression shown, since V_{IN} is 1V.

This circuit is most useful where a single spot frequency is desired and a fixed R-C combination can be selected. For example, with C_t of 1000pF, an R_t of 1kΩ will yield 100kHz as shown. For lower frequencies R_t can easily be adjusted upward; for example when it is 1MΩ, 100Hz will be produced. The nomograph of 22a1 is useful in selecting R_t values for various frequencies; not only for a C_t value of 1000pF, but for other values as well. Another example is 0.01µF and 100k, which yields 100Hz. It is



b. 10/1 Manually-Tuned Clock Generator



c. Self-Biasing Precision Clock

Figure 22. Clock Circuits

possible to use C_t values below 1000pF, or R_t values above 1MΩ. The tradeoff is simply that some predictability will be sacrificed in doing so. This nomograph is based on a fixed V_{IN} of 1V and is generally applicable to other circuits with such operating conditions. Examples are the two circuits which immediately follow.

With a little more effort, the same circuit can be adapted for manual tuning and switched capacitors. The circuit of Figure 22b provides this, with smooth tuning over a 10/1 range.

Here the simple 1V supply divider of Figure 22a is replaced by an LED reference circuit which improves supply stability and adds coarse temperature compensation for the diode drift. One volt is developed at the emitter of Q1 and drives the linear frequency control R2. Note that this low-cost circuit features utility with reasonable performance, but for the best TC an AD589 1.2V reference will be useful driving R2.

Resistors R4 and R5 here function as R_t, and the nominal value can be seen on Figure 22a1 with the various C_t values (see table). R5 serves to calibrate the circuit for full scale. For this circuit, a table of recommended C_t capacitor types are shown, including a preferred non-polar electrolytic hookup for low frequency (albeit non-precision) scale.

The previous two circuits are very strong on utility but as shown lack high precision and immunity to power supply changes. The clock circuit of Figure 22c improves on both of these weaknesses and adds an output buffer.

This circuit capitalizes on the fact that the AD654's internal quiescent current is regulated, and uses this current at pin 5 to excite a reference diode A2. This establishes a 1.235V reference, V_R, from pin 5 to common. This voltage is highly immune to supply changes, allowing the diode current to be stabilized without the expense of additional parts.

V_R also appears across R_t, and develops a timing current of V_R/R_t making the frequency expression as noted. The general frequency expression can be easily simplified so that the V_R and C_t factors divide out by making C_t a power of 1.2. This allows easy values for R_t, and also permits the use of the frequency nomograph 23a1 for R_t-C_t selection. To do so, simply multiply the capacitor curves as shown by 1.2 (1200pF, 12000pF, etc.) and select R_t. Of course the circuit will still need to be calibrated if exact frequency operation is needed. The output signal from pin 1 is not TTL compatible, but it is CMOS compatible with the use of a CMOS Schmitt buffer as shown. This restores a rail-rail 5V logic swing, which can drive either 5V CMOS, or TTL.

12-Bit D/F Converter

Closely allied to the clock sources, as well as standard V/F circuits is the D/F converter, a digitally programmed frequency source. A useful example of such a circuit is the 12-bit D/F shown in Figure 23.

This circuit uses the AD7240, a 12-bit resolution CMOS D/A available with differential nonlinearity as low as 1/2LSB. It is used here with the AD589 1.235V reference in

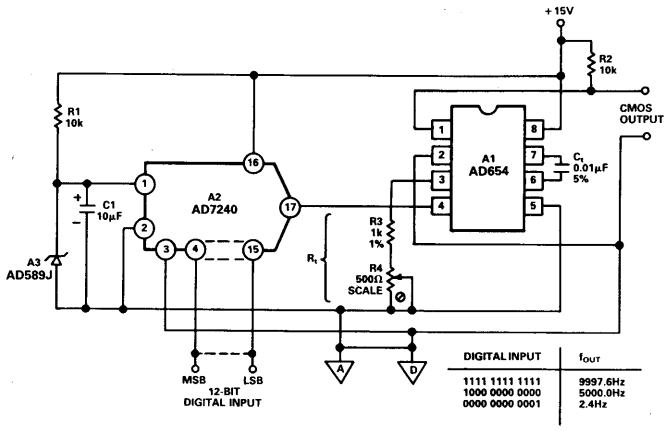


Figure 23. 12-Bit D/F Converter

a voltage output mode, driving the (+) input of the AD654 directly. Since the AD7240 is a multiplying D/A, it multiples the 1.2V reference by the fractional binary input, producing a variable voltage output similar to a pot. The AD654 is scaled here for a 1mA FS current; a C_t of 1000pF yields a FS output (for an "all ones" input) of 99976.Hz. The timing capacitor can be changed for other full scale frequencies. R_t is trimmed via R4 for FS calibration.

Nonlinearity error of this circuit will be predominantly due to the AD654 if the AD7240 is operated from a 15V supply as shown. Inasmuch as this circuit's linearity will be on the order of 0.1%, the best linearity grade for the AD7240 may not be cost effective. Nevertheless, the circuit will still be monotonic for 12-bits for all grades of the AD7240 and have 12-bits of control resolution. Similarly operated D/A devices of lower resolution can also be employed in this general circuit.

Voltage/Current Monitors

Using isolated V/F conversion techniques, a variety of useful voltage and current monitor circuits can be implemented. Several examples are shown in Figure 24.

In Figure 24a is a AD654 V/F scaled to measure a −5V bus, with a 1.0Hz/mV sensitivity. The output from the optoisolator is fed to one of the output buffers of Figure 10 (that is, 10a1 for example) to 5V TTL. While this example is for a 5V bus, a simple adjustment of the R1/R2 divider will allow other voltages. R5 should be selected for 9-10mA of drive in the LED.

Figure 24b illustrates a technique for monitoring negative supply current, in this case on a −20V bus. In this hookup, the negative voltage input mode is used with the V/F measuring the drop across R_S, a series sampling resistor.

In this circuit R1-R3 constitute R_t, and a value of R_S is selected from the table for the desired full scale current. In each case, the sense voltage is 100mV for minimum loss in the supply voltage. The capacitance C_N is a large value, selected for more than 25dB of noise attenuation. This circuit is scaled for the sensitivities shown in the table, and the nominal FS frequency is 1kHz.

A very interesting form of current monitor is shown in Figure 24c. This circuit is self powered and measures the

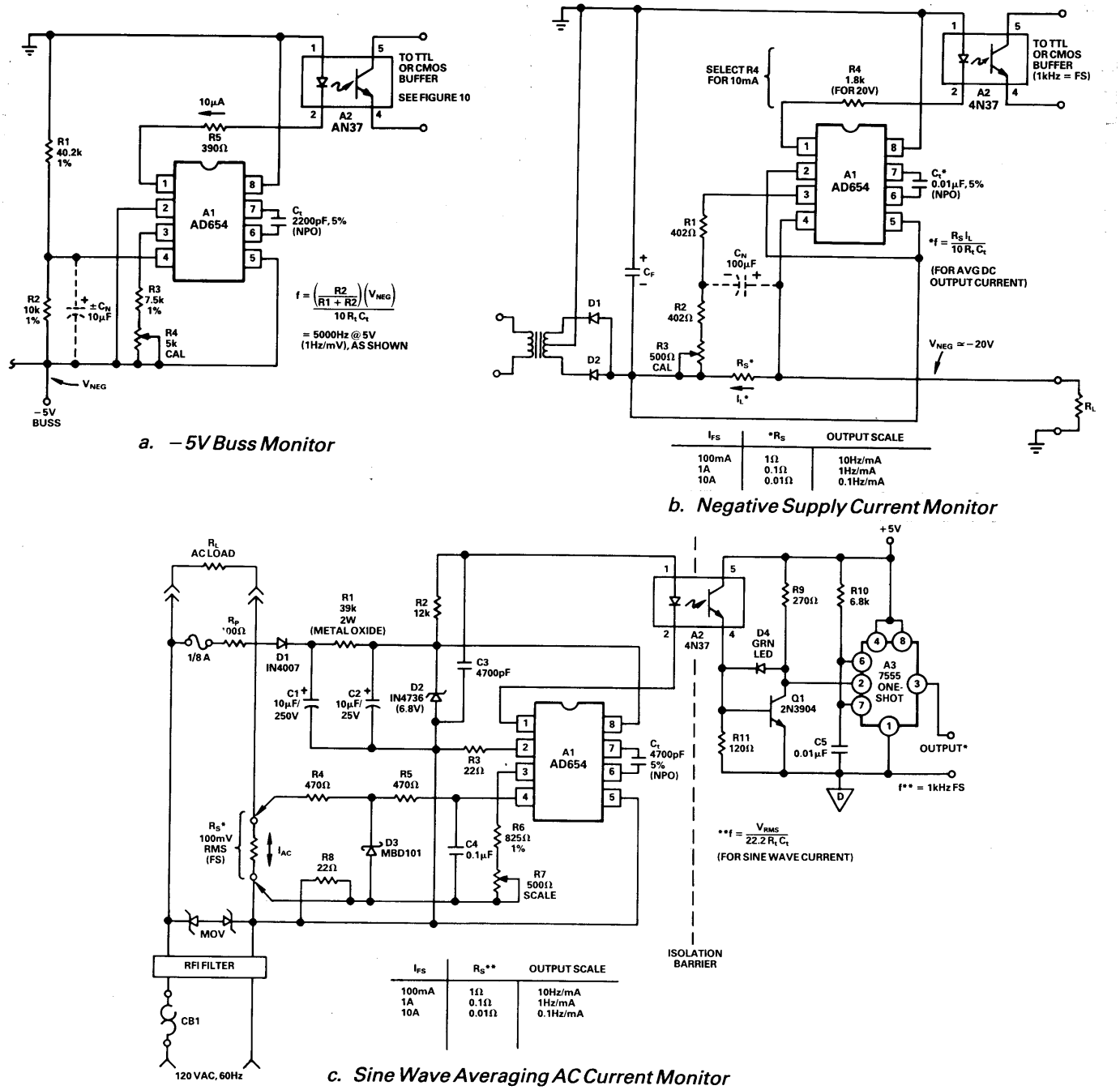


Figure 24. Voltage Current Monitors

average ac line current in the load R_L delivering an isolated output frequency. Several aspects of the circuit are similar to previous applications, such as the pulsed LED drive and the one shot regeneration (i.e., A2 and A3). They will not be discussed extensively here.

The circuit samples the current in R_S by measuring the ac terminal voltage. This is possible with an AD654 if the p-p ac input is only a few hundred mV. The AD654 simply half wave rectifies the ac and then measures the dc average over ½ cycle. Of course the input must be protected against overvoltage, thus the use of D3. C4 is simply a hash filter.

With a 100mV rms FS drop across R_S, the circuit is scaled to produce the frequency noted, 1kHz FS. R_S is selected for various FS currents, so as to produce 100mV rms. Note that since this is an average responding ac measurement, nonsinusoidal currents will not read correctly. For such applications, an rms-dc converter can be used, such as the AD636.

The circuit can be either line powered by a peak detector circuit and series resistor (D1, C1, R1), or can be fed from a small rectifier transformer and simple half-wave supply. The supply as shown functions adequately, but it is not efficient from a power consumption standpoint. When working with circuits operated directly from the line, it is of paramount importance that adequate safety precautions be taken. This would include safety and reliability considerations such as overvoltage clamps, breakers, sufficient derating, etc.

Although the circuit as it is shown measures current, it can also be rewired to measure line voltage by adding a divider so as to produce 100mV rms ac at R4.

High Input Impedance Bipolar V/F

A more precise bipolar V/F with a parallel sign bit output is shown in Figure 25. This circuit uses a low offset voltage, low bias current precision FET input op amp preceding the AD654. This allows operation from very high impedance sources and can achieve very accurate conversion down to millivolt levels with good symmetry about zero. The circuit operates from conventional ± 15V power supplies.

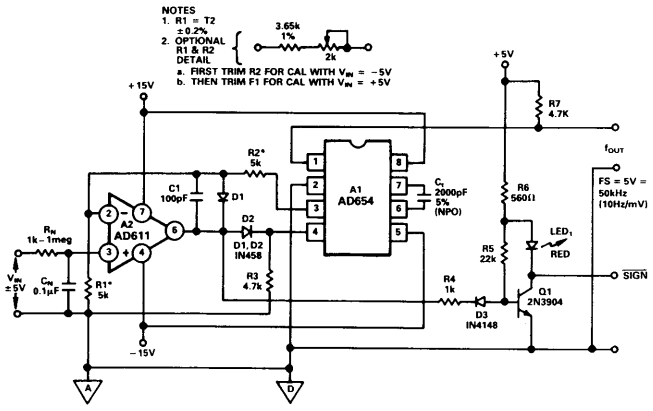


Figure 25. Ultra High Input Impedance Bipolar V/F

In this rather unusual circuit the AD654 is alternately driven in one of its two voltage input modes for the two input polarities. It acts as a positive input voltage V/F (for "positive" signal inputs), and as a negative input voltage V/F (for "negative" signal inputs). A2 is a low input current precision op amp which loads the source with only 10pA of bias current (typical). Low leakage diodes D1 and D2 provide switching at the AD654's inputs, while the precision resistors R1 and R2 set the V/F scale in conjunction with timing capacitor C_t.

Since R2 sets the scale factor for "negative" inputs, and R1 for "positive" inputs, gain calibration can be a bit complex. The most expeditious means of FS calibration is via software, with a known reference input, a fixed C_t, and a closely matched R1-R2. Alternately, C_t can be made 2200pF and R1-R2 trimmed, as noted. The scaling with the values shown is 50kHz for a FS V_{IN} of 5V (or 10Hz/mV), and excellent linearity is achieved for inputs down to 1mV or less. For best accuracy around zero a low offset device should be used for A2, such as the AD611K (500μV max), or A2 should be trimmed.

The circuitry around Q1 is a sign amplifier and produces a TTL compatible SIGN output as well as LED visual indication. Aside from the high precision of this circuit as a bipolar input V/F, the input buffer technique used is also useful for many single polarity sources which might require minimal loading, or the addition of long-time constant input filters.

Log Controlled Oscillator

For manually tuned oscillator applications, the widest range of control comes about with a logarithmic control characteristic. However, a log taper pot with a repeatable 4 decade characteristic is not a real-world item. A better approach is to use a linear pot fed into an exponential control circuit. This has the practical effect of a log control characteristic with a standard pot taper, but one not sensitive to the control's absolute value.

Figure 26 is a log controlled oscillator using the AD654 in conjunction with a dual op amp and a monolithic IC array. The array uses the same general principle discussed above with the Figure 21 function generator, but with some enhancements.

The lower part of the circuit is simply a hot substrate stabilizer for the plastic packaged CA3046 array. Q5 of the array is a diode connected sensor and Q3-Q4 the heaters. The V_{BE} of Q5 is compared against 650mV derived from the +15V supply; the loop forces the chip temperature upwards to about 40°C. This is only slightly in excess of room temperature, but more importantly it will be *constant*. The constant temperature removes the strong temperature sensitivity of the basic exponential generator, Q1-Q2, and it avoids the necessity of a special TC compensation resistor.

The current generator is composed of Q1 and Q2 with Q1 establishing a reference V_{BE} proportional to the current established by the reference diode A2 and R2-R3. R2 is trimmed to set this current to a nominal 500μA, but also to trim out circuit tolerances. With a C_t of 470pF this produces a 100kHz frequency.

The lower end of the operating range is established by the divider across Q1, R6-R8. R8 drops a voltage which is adjusted to be equal to 4 (KT/q ln 10), or about 240mV, as set by R6 for low scale calilbration. With R9 in shunt with R8, a sweep of this control spans 4 decades of current, controlling the oscillator over 4 decades.

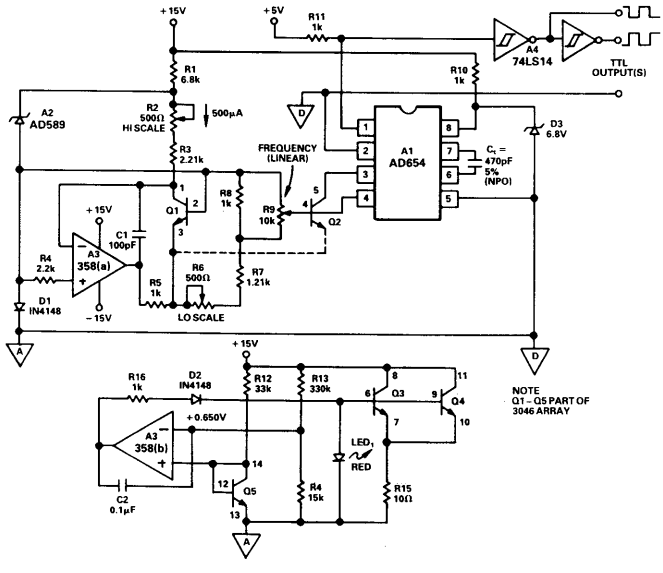


Figure 26. Log Controlled Oscillator 10Hz – 100kHz

Frequency Doubling

Since the AD654's output is a square-wave rather than a pulse train, information about the input signal is carried on both halves of the output waveform. The circuit in Figure 27 converts the output into a pulse train, effectively doubling the output frequency, while preserving the

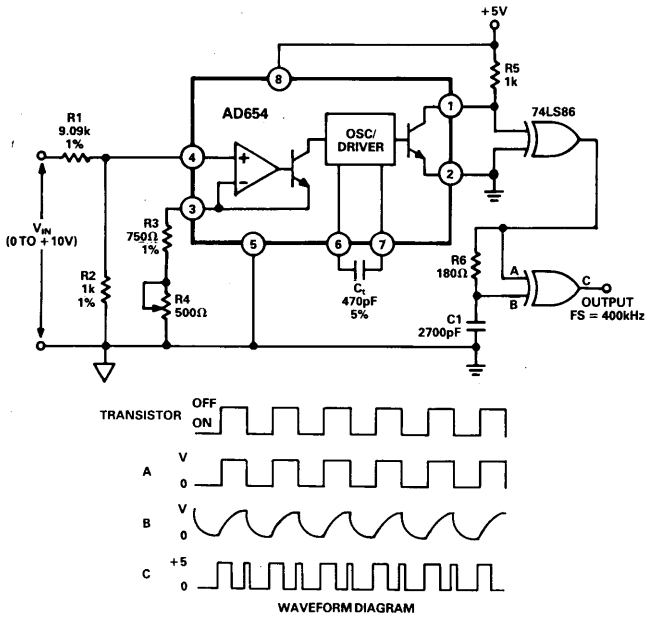


Figure 27. Frequency Doubling

better low frequency linearity of the AD654. This circuit also accommodates an input voltage that is greater than the AD654 supply voltage.

Resistors R1–R2 are used to scale the 0 to +10V input voltage down to 0 to +1V as seen at pin 4 of the AD654. Recall that V_{IN} must be less than V_{SUPPLY} −4V, or in this case less than 1V. The timing resistor and capacitor are selected such that this 0 to +1V signal seen at pin 4 results in a 0 to 200kHz output frequency.

The use of R6, C1 and one XOR gate doubles this 200kHz output frequency to 400kHz. The voltages seen at the input of the second section of the 74LS86 are shown in the waveform diagram. Due to the difference in the charge and discharge time constants, the output pulse widths of the 74LS86 are not equal. The output pulse is wider when the capacitor is charging due to its longer rise time than fall time. The pulses should therefore be counted on their rising, rather than falling, edges.

2MHz, Frequency Doubling V/F

Operation of the AD654 via the conventional output (pins 1 & 2) is speed limited to approximately 500kHz for reasons of TTL logic compatibility. However, even though the output stage of the device may become speed limited at this output the multivibrator core itself will still continue to oscillate to 1MHz or more. Advantage can be taken of this feature to allow even higher frequencies of operation then might be expected, frequencies well in excess of 500kHz. To implement such an "exalted" mode, a basically different signal extraction method is used. Rather than using the internal output stage the timing capacitor signal is buffered and zero crossing level detected to produce a high speed, TTL square wave output.

Figure 28 is a circuit example of this type of operation illustrating a 2MHz full scale V/F. In this circuit, the AD654 is operated at a FS of 1mA with a C_t of 100pF. This achieves a basic device FS frequency of 1MHz across C_t. The P channel JFETs Q1 and Q2 buffer the differential timing capacitor waveforms to a low impedance level where the push-pull signal is then ac coupled to the high-speed comparator A2, an LM360 (or μA760). This device has a low delay of 12ns (typical), and push-pull TTL outputs. Hysteresis is used, via R7, for nonambiguous switching and to eliminate the oscillations which would otherwise occur at low frequencies. While the value of this resistor is not critical, it must *not* be omitted. Without the hysteresis the circuit will generate spurious output frequencies and simply be uncontrollable.

The net result of the above is a very high-speed circuit which does not compromise the AD654 low scale dynamic range as the FET buffers will typically have only a few pA of bias current. At the other extreme, the high end

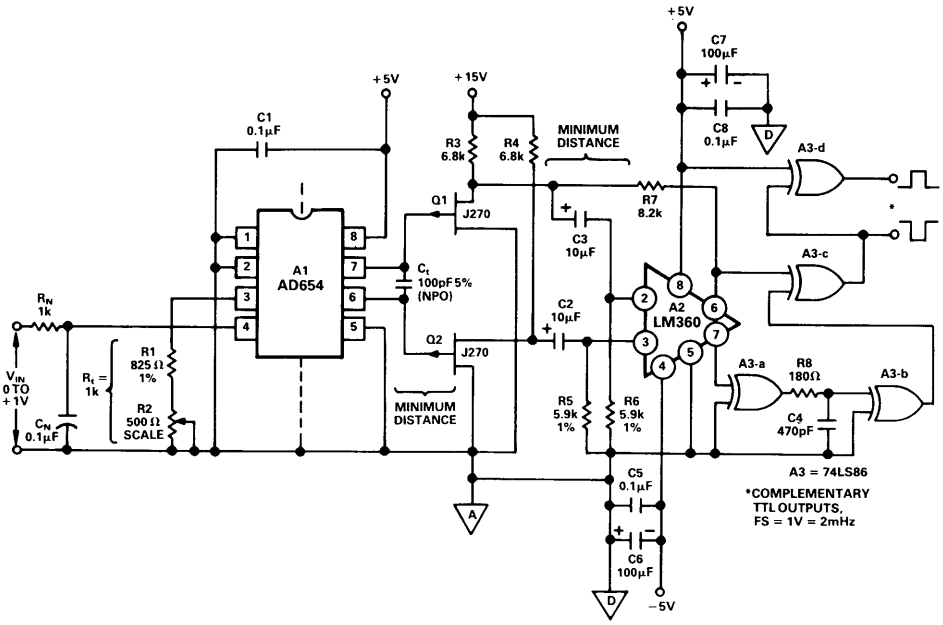


Figure 28. 2MHz, Frequency Doubling V/F (Exalted Mode)

dynamic range is limited essentially by the AD654 parasitic package and layout capacitances in shunt with C_t, and also those from each node to ac ground. A tight, minimum lead length PC layout will help between A1-6/A1-7 and Q1/Q2. When constructed properly the circuit is capable of stable operation to frequencies higher than 1MHz. A ground plane will also help stability, connnected to analog ground at one point. Low impedance bypasses on all supplies are also needed, as noted.

The output of the comparator is a complementary square wave at 1MHz FS. The XOR gate following A2 acts as an edge detector, producing a short (≈50ns) pulse for each input state transition. This effectively doubles the V/F FS frequency to 2MHz with complementary logic outputs at gates A3-c and A3-d. Note that this frequency doubler technique is not at all unique to this particular V/F circuit; it can be applied to a number of other circuits in this note as well.

The final result is a 1V FS input V/F with a 2MHz FS output capability. The increased dynamic range and speed of this circuit can open up many additional categories of applications. For example, wider data bandwidths can now be handled by the V/F since the operating frequency is about an order of magnitude higher than is standard. High speed data communications and video are two examples.

Interestingly, while the linearity related error of this circuit is not as good as it might be if the V/F were to be operated at 100kHz, the relative degradation is actually much less than the frequency scaling would suggest. For example, while a 100kHz scaled V/F might have a nonlinearity on the order of 0.1%, this circuit has a typical nonlinearity of about of 0.5% (or less). This level of performance is useful for many types of applications, particularly so in view of the low cost.

REFERENCES:

1) Gilbert, B.A. "A Versatile Monolithic Voltage-to-Frequency Converter," *IEEE Journal of Solid-State Circuits*, vol SC-11, pp. 852-864, Dec. 1976.

2) Kress, D.; Gilbert, B.A. "Versatile Monolithic V/f or I/f Converter," *Analog Dialogue*, vol 10-2, pp. 6-8, 1976.

3) Jung, W.G. *IC Op Amp Cookbook, 2nd Edition*, Howard W. W. Sams and Co. Inc, Indianapolis, 1980.

4) Jung, W.G. *IC Timer Cookbook, 2nd Edition*, Howard W. Sams and Co. Inc, Indianapolis, 1983.

5) Jung, W.G. "V/F Converter Doubles as Clock and Input of Stable Sine-wave Source," *Electronic Design*, pp. 328, November 15, 1984.

6) Gilbert, B.A. "Monolithic Analog Trigonometric Function Generator," *Analog Dialogue*, vol 18-3, pp. 12-14, 1984.

7) DeVito, L.M. "AD650 Data Sheet," Analog Devices

8) Gardner, F.M. *Phase Lock Techniques, 2nd Edition*, Wiley, 1979.

SPECIAL SOURCES

Listed below are some manufacturers of specialty electronic components useful within V/F circuits.

Manufacturer:	**Component(s):**
Corning Glass Works 3900 Electronics Drive Raleigh, NC, 27604 (919)-876-1100	NPO (COG) Ceramic Caps Types CAC02/03/04/05
F-Dyne Electronics 449 Howard Ave. Bridgeport, CT, 06605 (203)-367-6431	Polystyrene Caps Type PJ (See Also PSA, PST Types)
Optoelectronics Division General Instrument Corp. 3400 Hillview Ave. Palo Alto, CA, 94304 (415)-493-0400	4N137, 6N135/6N136 (See Also Phototransistors, Photodiodes, and LEDs)
Tel-Labs, Inc. 154 Harvey Road P.O. Box 375 Londonderry, NH, 03053 (603)-625-8994	WW and Metal Film Resistors (See Also Special Linear, Pos TC Resistors; +140ppm/°C)