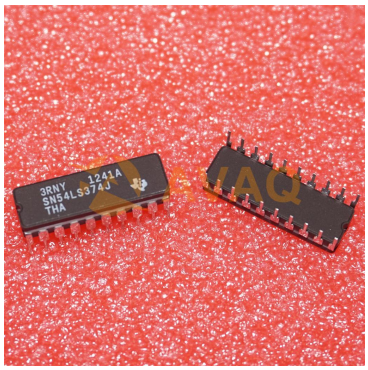
SN54LS374J

Flip Flop D-Type Bus Interface Pos-Edge 3-ST 1-Element 20-Pin CDIP Tube

Manufacturer:	Texas Instruments, Inc
Package/Case:	CDIP20
Product Type:	Logic ICs
Lifecycle:	Active



Images are for reference only

Inquiry

General Description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ’LS373 and ’S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the ’LS374 and ’S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the ’S373 and ’S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control (OC) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OC\ does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

Key Features

Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package

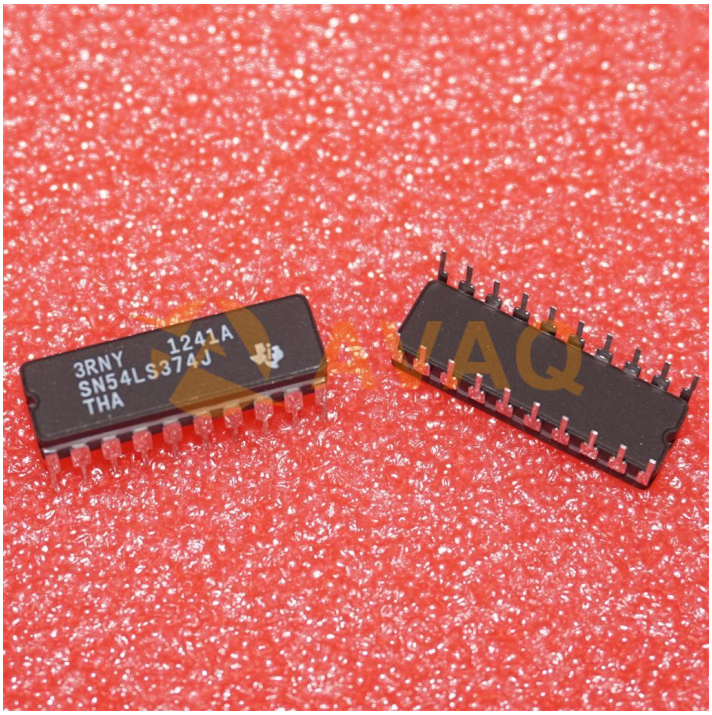
3-State Bus-Driving Outputs

Full Parallel Access for Loading

Buffered Control Inputs

Clock-Enable Input Has Hysteresis to Improve Noise Rejection (’S373 and ’S374)

P-N-P Inputs Reduce DC Loading on Data Lines (’S373 and ’S374)



Recommended For You

SN74S38N

Texas Instruments, Inc

DIP

SN7438N

Texas Instruments, Inc

DIP14

SN75462P

Texas Instruments, Inc

DIP8

SN74F08D

Texas Instruments, Inc

SOP-14

SN74LS257BN

Texas Instruments, Inc

DIP16

SN75452BP

Texas Instruments, Inc

DIP8

SN74LS245DW

Texas Instruments, Inc

SOP20

SN74LS74AN

Texas Instruments, Inc

DIP

SN74S74N

Texas Instruments, Inc

DIP

SN7406N

Texas Instruments, Inc

DIP-14

SN74CBTLV3257D

Texas Instruments, Inc

SOP-16P

SN74HC138DR

Texas Instruments, Inc

SOP16

SN74LS14N

Texas Instruments, Inc

DIP

SN74HC139N

Texas Instruments, Inc

DIP

SN74AVC16T245DGGR

Texas Instruments, Inc

TSSOP48