Application Brief

Power Supply Design for Horizon Robotics Journey 5

This application brief details the design considerations of the power design for the Horizon Robotics Journey 5(J5) system-on-chip (SoC) power rails using two TPS6594-Q1 power management integrated circuits (IC) and six TPS62873-Q1 synchronous buck converters. The original power source is the battery. A reverse-protection LM74700-Q1 device is used between the LM5143-Q1 input and the battery. The power input on this design is the 5-V bus from the LM5143-Q1 dual-synchronous buck output. All components in this design are automotive qualified.

The TPS6594-Q1 IC has five buck converters. The two TPS62873-Q1 buck converters are stackable for a high current requirement core and battery protection unit (BPU). This power-management IC (PMIC) is non-volatile memory (NVM) programmable, meaning the default register values are set in the TI production line to the desired values for this platform without further need for the customer to change settings. The full orderable part numbers for this OTP spin are TPS6594C31RWERQ1 for PMIC-A and TPS6594C41RWERQ1 for PMIC-B, shown in the block diagram.

This power design exhibits how the required rails for J5 can be powered with TI PMICs. A designer can customize and optimize their power needs based on the actual use case regarding a SoC variant, current requirements, used peripherals, and so forth. The designer can also use the I2C bus for diagnostic testing and other control of this PMIC.

Design Parameters

Table 1 shows the power rails, load requirements, maximum ramp rate, and power group.

Table 1. Design Parameters

Power Rail	Voltage (V)	Current (A)	Maximum Ramp Rate (mV/µs)	Power Group
VDD_CORE	0.8	24	< 18	5
VDD_BPU0	0.8	26.5	< 18	7
VDD_BPU1	0.8	26.5	< 18	7
VDDQ_DDR0	1.1	3.4	< 5	4
VDDQ_DDR1	1.1	3.4	< 5	4
VDD_DDR0	0.8	3.9	< 18	6
VDD_DDR1	0.8	3.9	< 18	6

Table 2 shows the power rails, load requirements, maximum ramp rate and power group.

Table 2. Digital Power

Power Rail	Voltage (V)	Current (A)	Maximum Ramp Rate (mV/µs)	Power Group
VDDIO_SD_1V8	1.8	3.8	< 18	1
VDDIO_SD_3V3	3.3	1.4	< 18	1
VDDIO_SD_SD1	3.3/1.8	0.13	< 18	1
VDDQ_AO	0.8	0.55	< 18	2

Table 3 shows the power rails, load requirements, maximum ramp rate and power group.

Table 3. Analog Power

Power Rail	Voltage (V)	Current (A)	Maximum Ramp Rate (mV/µs)	Power Group
VAA_DDR_1V8	1.8	0.02	< 5	3
VPH_PCIE_1V8	1.8	0.07	< 180	3
VDDIO_PVT_1V8	1.8	0.01	< 18	3
VP_PCIE_0V8	0.8	0.14	< 80	5
VQPS_EFUSE_1V8	1.8	0.08	< 18	6
VPH_MIPI_1V8	1.8	0.06	< 100	8
VPH_MIPI_0V8	0.8	0.15	< 100	8

Power Design

Figure 1 shows a block diagram using the TPS6594-Q1, TPS62873-Q1, and LM5143-Q1 devices powering the J5 SoC power rails.

Main features:

- Power sequencing for J5 rails are controlled with PMIC TPS6594-Q1
- The PGOOD signals act as the nRESET signal for the SoC
- An interrupt signal can be used for fault detection
- The 3 GPIO outputs on the TPS6594-Q1 device can be used to control the TPS62873-Q1 device for power sequencing

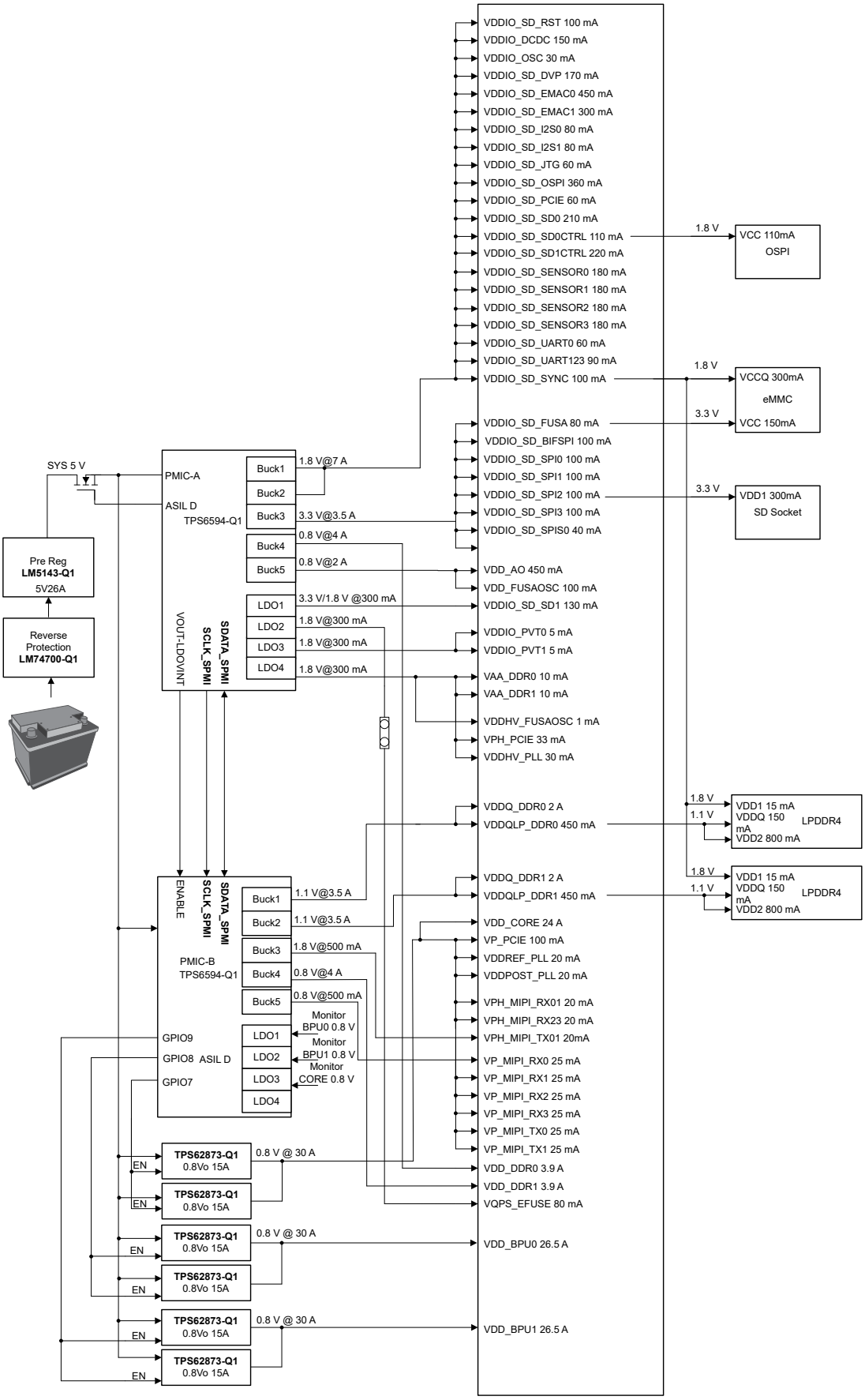

Figure 1. J5 Power Design Block Diagram

Power-Up Sequencing

Figure 2 shows an example power-up timing of the power rails and power group corresponding signals.

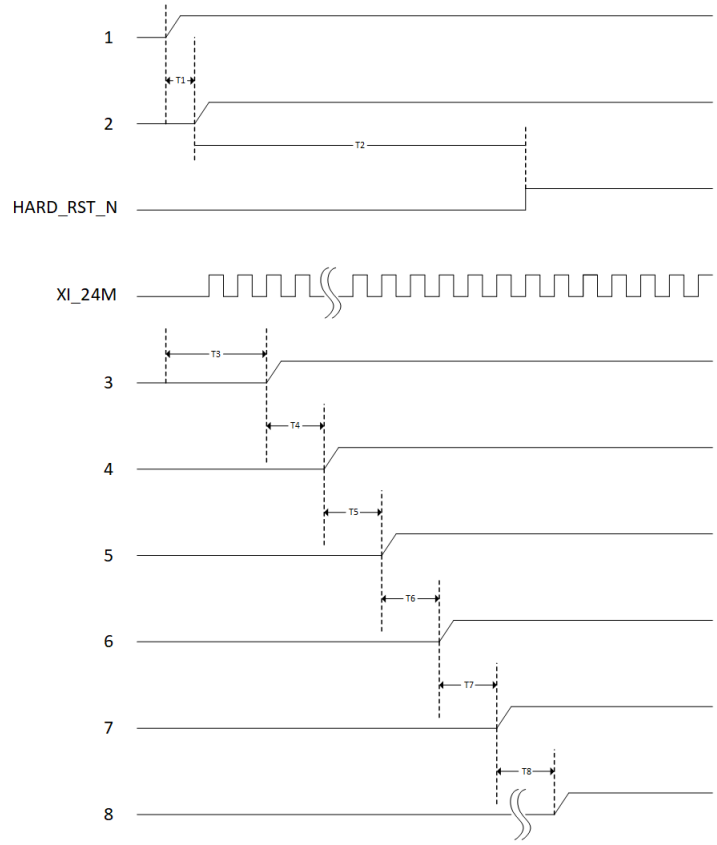

Figure 2. Power-Up Sequencing

Power-Down Sequencing

Figure 3 shows an example power-down timing of the power rails and power group corresponding signals.

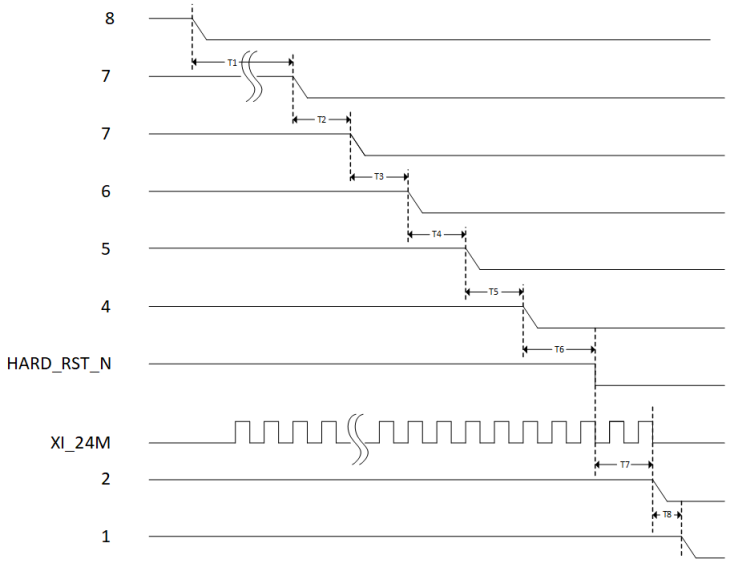

Figure 3. Power-Down Sequencing

Schematic

Figure 4 shows the TPS6594-Q1 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide. For LDO input and output capacitor values, see the data sheet recommendation.

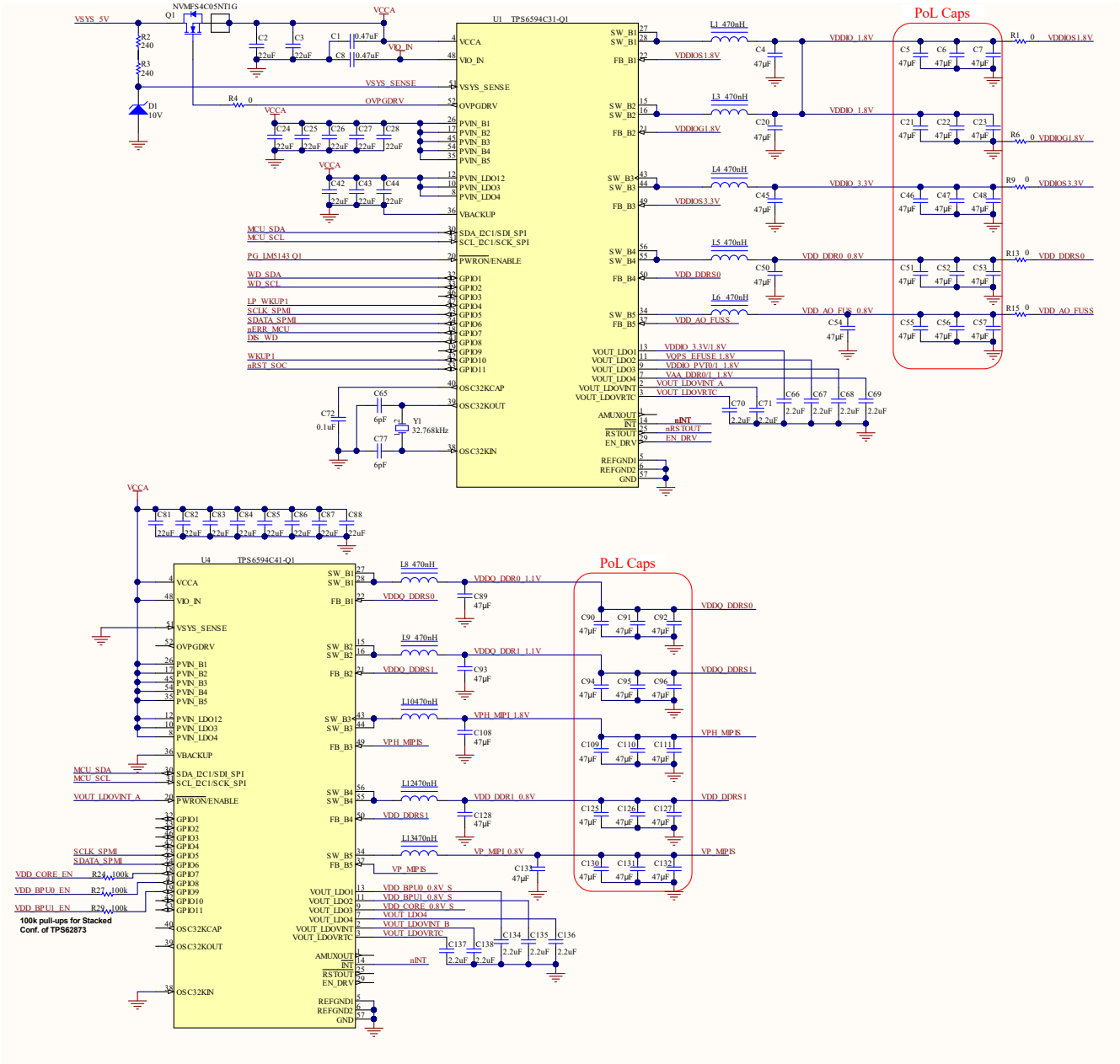

Figure 4. TPS6594-Q1 Schematic

Figure 5, Figure 6, and Figure 7 show the TPS62873-Q1 schematic with critical components. For layout guidance, see the corresponding device data sheet and EVM user guide.

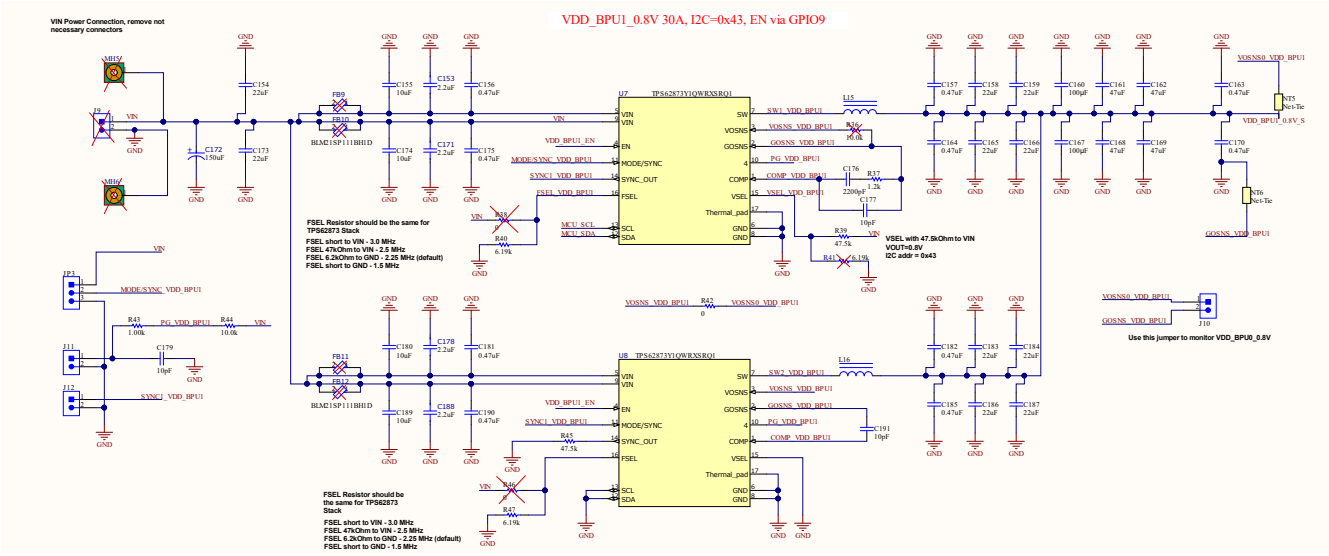

Figure 5. TPS62873-Q1 Schematic for VDD_BPU1

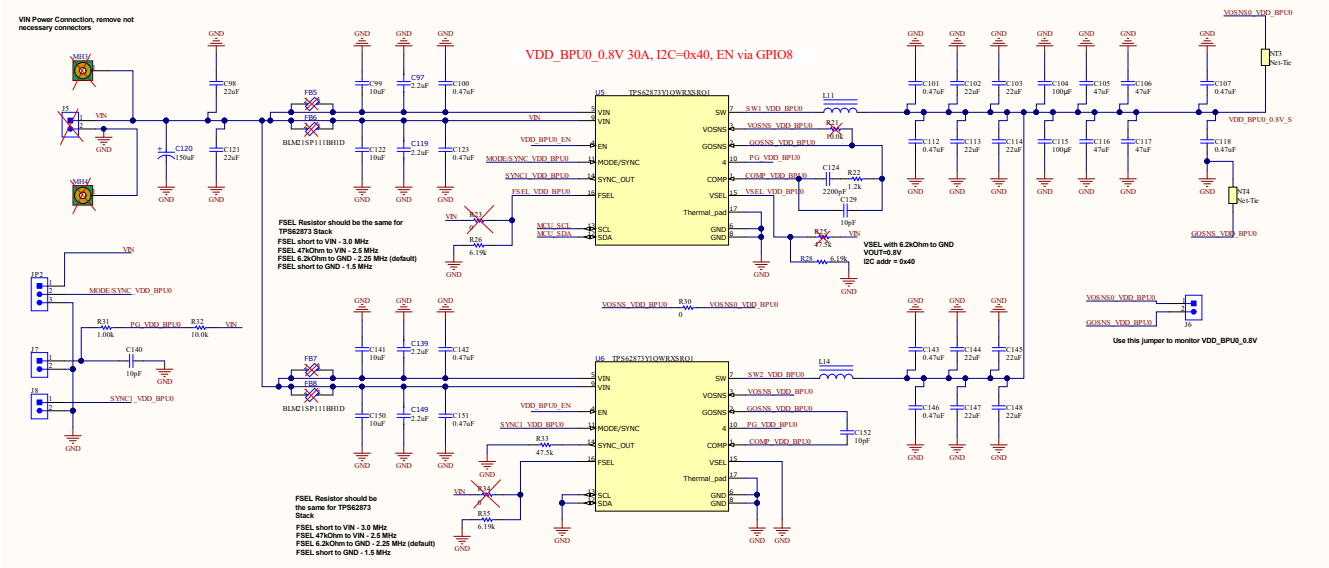

Figure 6. TPS62873-Q1 Schematic for VDD_BPU0

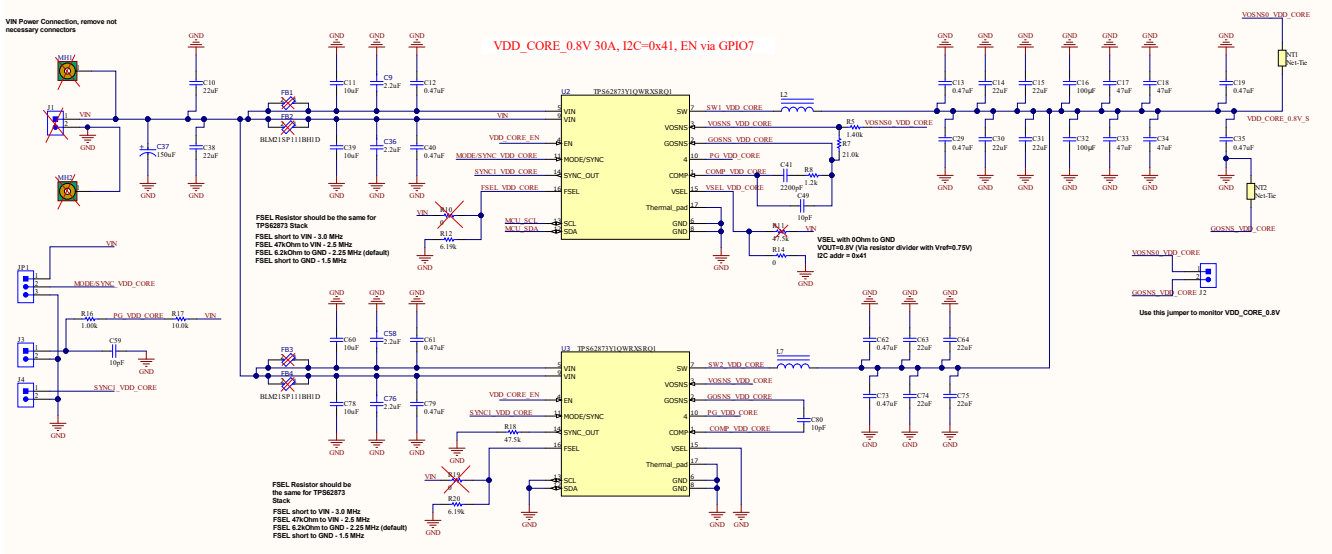

Figure 7. TPS62873-Q1 Schematic for VDD_CORE

Summary

The design outlined in this application brief, using the TPS6594-Q1, TPS62873-Q1, and LM5143-Q1 ICs, provides the power requirements for Horizon Robotics Journey 5 SoC while maintaining good efficiency. This design is compact, due to the minimum number of external components. The I2C control allows for diagnostic testing and other control of the TPS6594-Q1 device.

References

1. Texas Instruments, *TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications* data sheet
2. Texas Instruments, *TPS6287x-Q1 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Automotive, Stackable, Synchronous Step-Down Converters with Fast Transient Response* data sheet
3. Texas Instruments, *LM5143-Q1 Automotive 3.5-V to 65-V Dual Synchronous Buck Controller With Low I_Q* data sheet
4. Texas Instruments, *LM74700-Q1 Low I_Q Reverse Battery Protection Ideal Diode Controller* data sheet

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