DC1220B QUICK START GUIDE

LTC3225EDDB

Low Profile Regulated Dual Cell SuperCAP Charger

DESCRIPTION

Demonstration circuit DC1220B is a Low Profile Regulated Dual Cell SuperCAP Charger featuring the LTC3225. The LTC3225 is a constant-current SuperCAP charger designed to charge two SuperCAPs in series to a fixed output voltage of 4.8V/5.3V from a 2.9V to 5.5V input supply. Automatic cell balancing is achieved during the charging phase.

Low input noise, low quiescent current and low external parts count make the LTC3225 ideally suited for small, battery-powered applications. Charging current level is programmed through an external resistor. Internal current limit and thermal shutdown circuitry allows the part to survive a continuous short-circuit from PROG to GND. When the input supply is removed, the LTC3225 automatically enters a low current state, drawing less than 1µA from the SuperCAPs.

The LTC3225 is offered in a 10-lead (3mm × 2mm) DFN package.

Design files for this circuit board are available. Call the LTC factory.

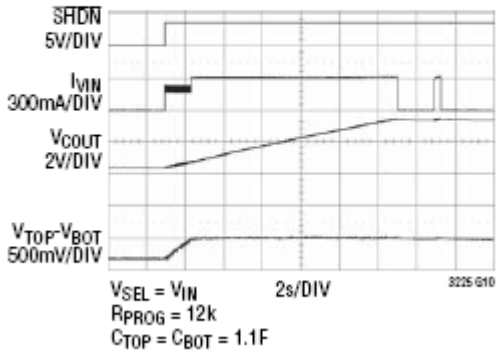
TABLE 1. TYPICAL SPECIFICATIONS (25°C)

Input Voltage Range: V_{CC}	2.9V to 5.5V
Charge Current	30mA or 150mA dependant on JP3 setting
VOUT	4.8V or 5.3V dependant on JP2 setting

OPERATING PRINCIPLES

The LTC3225 is a dual cell SuperCAP charger using a constant-current/constant-voltage algorithm. Its ability to control input charge currents up to 300mA and achieve automatic cell balancing during charging makes it well suited for charging two series connected SuperCAPs. The LTC3225 includes an internal switched capacitor charge pump to boost Vin to a regulated output voltage. A unique architecture maintains relatively constant input current for the lowest possible input noise. The basic charger circuit requires only three external components.

Charging Profile with Unequal Initial Output Capacitor Voltage (Initial V_{TOP} = 1V, V_{BOT} = 1.3V)



QUICK START PROCEDURE

Using short twisted pair leads for any power connections and with all loads and power supplies off, refer to Figure 1 for the proper measurement and equipment setup.

1. Jumper and Load Settings to start:
   JP1 (RUN) = SHDN
   JP2 (VOUT SELECT) = 5.3V
   JP3 (Iin LIMIT) = 30mA
   LOAD1 = off
2. Set VIN to 3.0V and verify that the input current is less than 10mA. Verify that VOUT is less than 3.8V indicating that the SuperCAP is in a low charge state.
3. Set JP1 to the RUN position. Verify that the input current is ~60mA. Verify that VOUT is less than 4.0V and that PGOOD is low.
4. Monitor PGOOD and VOUT. When PGOOD goes high, verify that VOUT is ~5.0V.
5. Verify that VOUT is ~5.3V when the input current drops to less than 10mA indicating a fully charged capacitor.
6. Turn on Load1 and set to 50mA. Monitor PGOOD and VOUT. When PGOOD goes low, verify that VOUT is ~4.9V.
7. Set JP1 to SHDN and allow the SuperCAP to discharge to 1.5V at which point Load1 will be set to 0mA and turned off.
8. Set JP3 to 150mA
9. Set JP1 to the RUN position. Verify that the input current is ~300mA. Verify that PGOOD is low.
10. Monitor PGOOD and VOUT. When PGOOD goes high, verify that VOUT is ~5.0V.
11. Verify that VOUT is ~5.3V when the input current drops to less than 10mA indicating a fully charged capacitor.
12. Turn on Load1 and set to 200mA. Monitor PGOOD and VOUT. When PGOOD goes low, verify that VOUT is ~4.9V.
13. Set JP1 to SHDN, increase Load1 to 500mA and allow the SuperCAP to discharge to 1.5V at which point Load1 will be set to 0mA and turned off.
14. Set JP2 to 4.8V
15. Set JP1 to the RUN position. Verify that the input current is ~300mA. Verify that PGOOD is low.
16. Monitor PGOOD and VOUT. When PGOOD goes high, verify that VOUT is ~4.55V.
17. Verify that VOUT is ~4.8V when the input current drops to less than 10mA indicating a fully charged capacitor.
18. Turn on Load1 and set to 200mA. Monitor PGOOD and VOUT. When PGOOD goes low, verify that VOUT is ~4.45V.
19. Set JP1 to SHDN, increase Load1 to 500mA and allow the SuperCAP to discharge to 1.0V at which point Load1 will be set to 0mA and turned off.

APPLICATION INFORMATION

This demo circuit is designed to demonstrate the full capability of the LTC3225 Low Profile Regulated Dual Cell SuperCAP Charger. Not all components are required in all applications. The critical circuit components are on the top of the board near the IC and listed in the Required Circuit Components section of the Bill of Materials, see Figure 4.

The style and value of the input capacitors C2 and C6 controls the amount of ripple present at the input pin (Vin). To reduce noise and ripple, it is recommended that a low equivalent series resistance (ESR) multilayer ceramic chip capacitor (MLCCs) be used. A 10nH inductor between C6 and C2 will reject fast cur-

rent notches thereby presenting a nearly constant load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with a PC board trace of 1 cm in length.

The amount of current drawn from VIN to charge the SuperCAP is programmed using a single resistor from the PROG pin to ground. The charge current (referred to VIN) is approximately 1600 times the current out of the PROG pin.

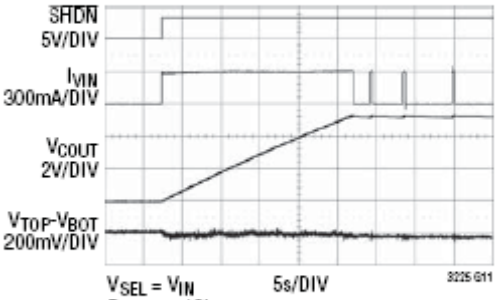
The power efficiency of the LTC3225 is similar to that of a linear regulator with an effective input voltage of twice the actual input voltage. In an ideal voltage doubler the power efficiency would be 50%. At moderate to high output power the switching losses and quiescent current of the LTC3225 are negligible thus this estimate of efficiency is valid.

The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary to have 0.6µF of capacitance for the flying capacitor. Ceramic capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. When comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specific capacitance value. For example, a 4.7µF 10V Y5V ceramic capacitor in a 0805 case may not provide any more capacitance than a 1µF 10V X5R or X7R ceramic capacitor in the same 0805 case. In fact the 1µF 10V X5R or X7R ceramic capacitor will provide more capacitance than the 4.7µF 10V Y5V ceramic capacitor. The manufacture's data sheet should be consulted to determine what value of capacitor is needed to ensure that the minimum capacitance values are met over the operating temperature and bias voltage.

Output voltage programming is accomplished by setting the VSEL pin either high or low. A high (VSEL> 1.3V) will set the output threshold voltage to 5.3V while a low (VSEL < 0.4V) will set the output threshold voltage to 4.8V.

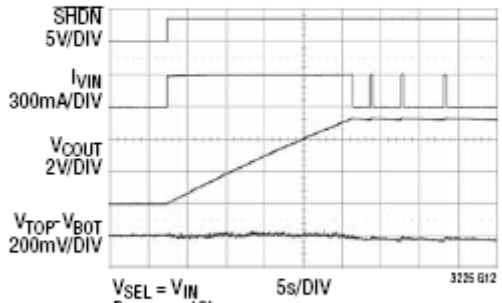
For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3225. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the GND pin (pin 8) and the exposed pad (Pin 11) of the DFN package to a ground plane under the device on two layers of the PC board can reduce the thermal resistance of the package and the PC board considerably.

Charging Profile with 30% Mismatch in Output Capacitance ($C_{TOP} > C_{BOT}$)



$V_{SEL} = V_{IN}$
$R_{PROG} = 12k$
$C_{TOP} = 1.43F$
$C_{BOT} = 1.1F$
C_{TOP} INITIAL VOLTAGE = 0V
C_{BOT} INITIAL VOLTAGE = 0V

Charging Profile with 30% Mismatch in Output Capacitance ($C_{TOP} < C_{BOT}$)



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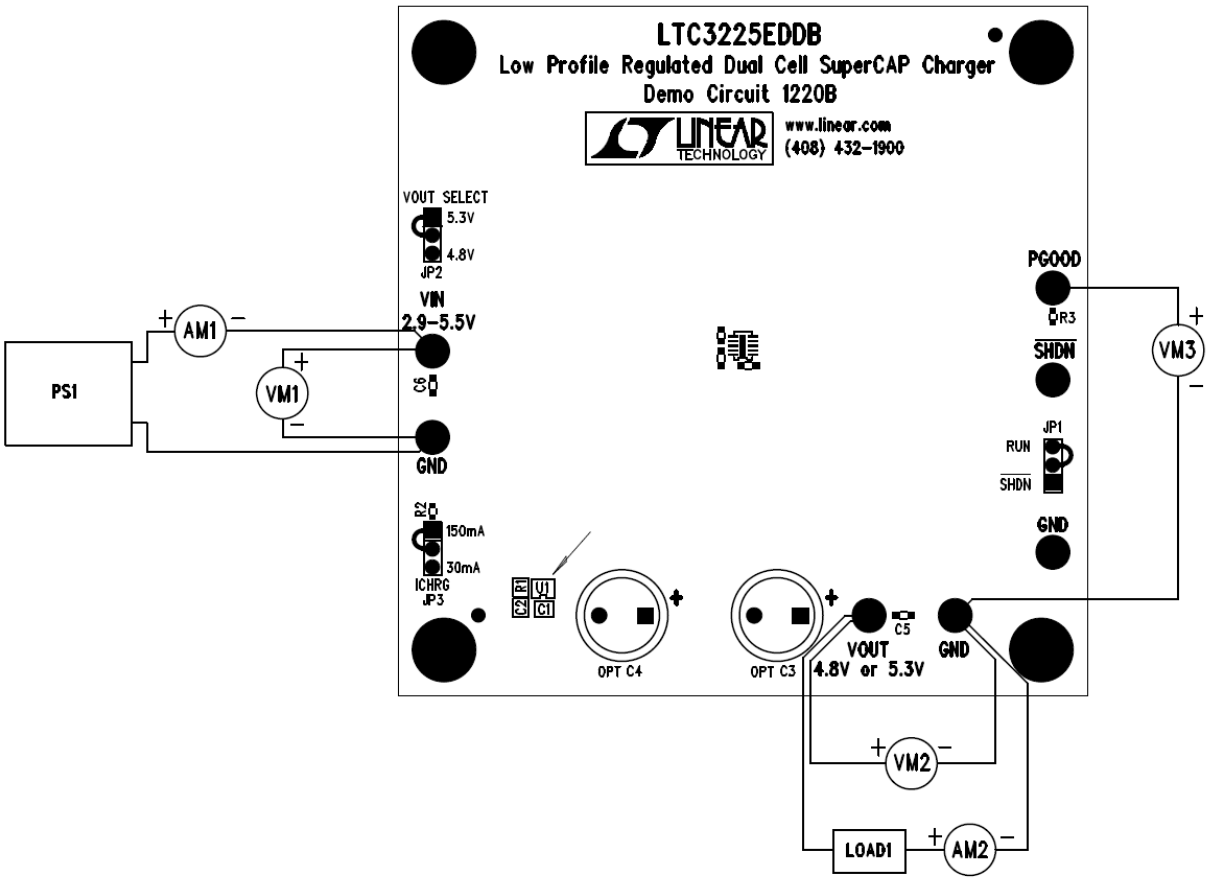

Figure 1. Proper Measurement Equipment Setup

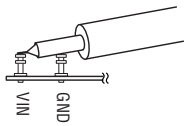

Figure 2. Measuring Input or Output Ripple

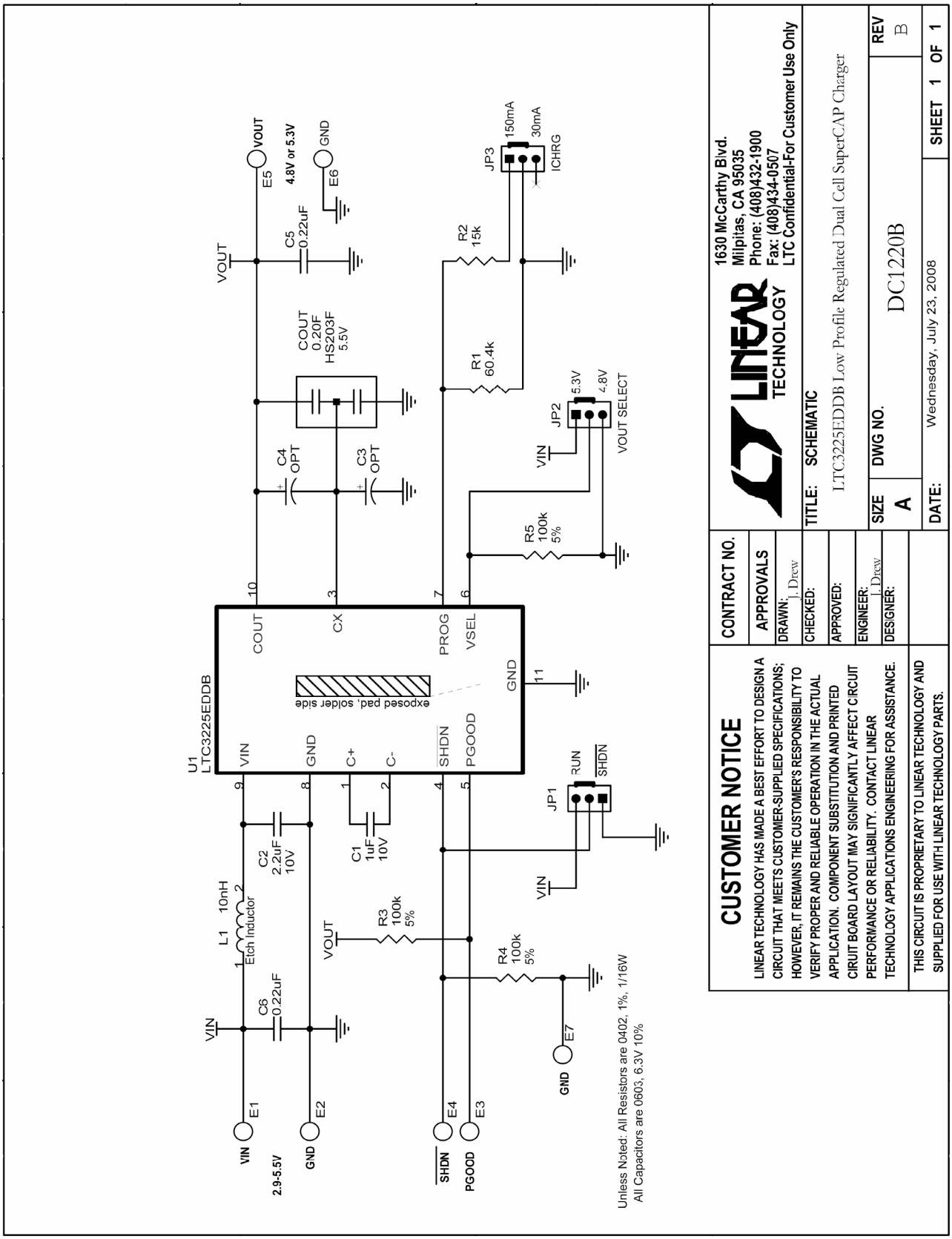

Figure 3. Circuit Schematic

Item	Qty	Reference - Des	Part Description	Manufacturer, Part #
REQUIRED CIRCUIT COMPONENTS:				
1	1	C1	CAP, CHIP, X7R, 1uF, 10% 10V, 0603	Murata, GRM188R71A105KA61D
2	1	C2	CAP, CHIP, X7R, 2.2uF, 10% 10V, 0603	Murata, GRM188R71A225KE15D
3	2	C5, C6	CAP, CHIP, X7R, 0.22uF, 10% 6.3V, 0603	Murata, GRM188R70J224KA88D
4	1	COUT	SUPERCAP, 0.20F, 5.5V	CAP-XX, HS203F
5	1	R1	RES, 60.4K OHM, 1%, 1/16W, 0402	VISHAY, CRCW040260K4FKED
6	1	R2	RES, 15K OHM, 1%, 1/16W, 0402	VISHAY, CRCW040215K0FKED
7	1	U1	Low Profile Regulated Dual Cell Super-CAP Charger	LTC3225EDDB
ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS:				
1	0	OPT-C3, OPT-C4	SUPERCAP 2.5V OR 2.7V	
2	3	R3,R4,R5	RES, 100K OHM, 5%, 1/16W, 0402	VISHAY, CRCW0402100KJNED
HARDWARE FOR DEMO BOARD ONLY:				
1	7	E1,E2,E3,E4,E5, E6, E7	TURRET, 0.09 DIA	MILL-MAX, 2501-2
2	3	JP1,JP2,JP3	HEADER, 3 PINS, 2mm	SAMTEC, TMM-103-02-L-S
3	3	JP1,JP2,JP3	SHUNT 2MM	SAMTEC, 2SN-BK-G
4	4		STAND-OFF, NYLON 0.375" tall (SNAP ON)	KEYSTONE,8832 (SNAP ON)

Figure 4. Bill of Materials