PF8200DB - NXP General

Configuration report for PF8200 OTP program ID: DB rev A

Rev. 1.3 — 31 October 2019 **Report**

1 General description

The PF8200 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32V based applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 2 qualified.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C after start up offering flexibility for different system states.

Note: Electrical characteristics are mantained in the PF8100_PF8200 data sheet

2 Features and benefits

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog monitoring
- Independent OV/UV monitoring circuits
- One-time programmable device configuration
- 3.4 MHz I^2C communication interface
- 56-pin 8 x 8 QFN package
- AEC-Q100 grade 2 qualified
- Safety mechanisms to fit ASIL B applications

3 Applications

- Automotive infotainment
- High-end consumer and industrial

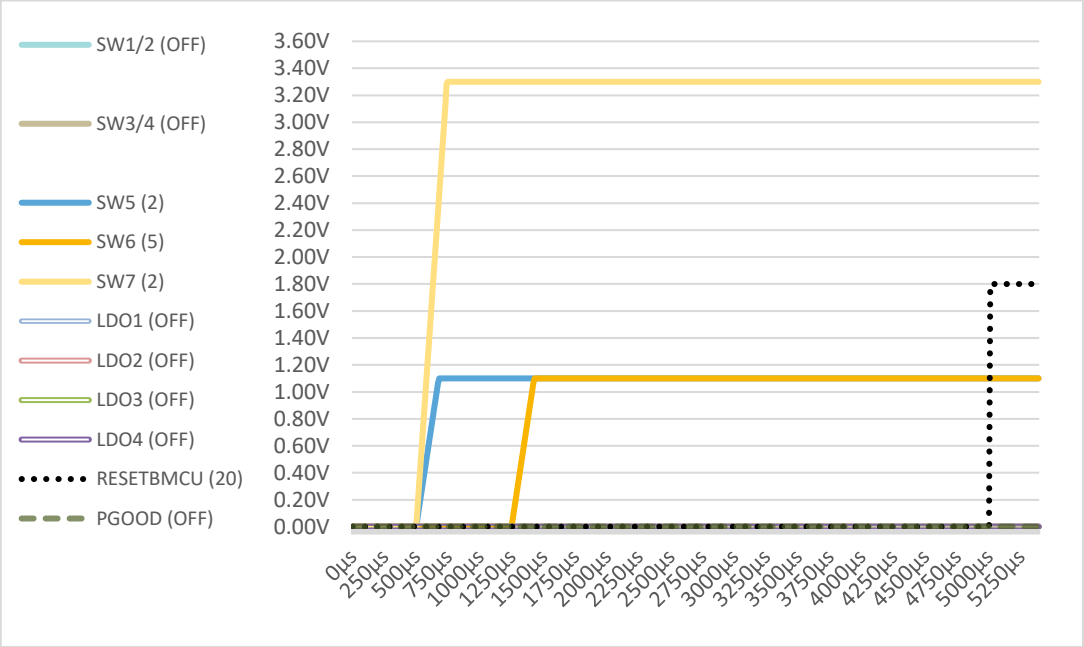
4 Ordering information

Table 1. Ordering information

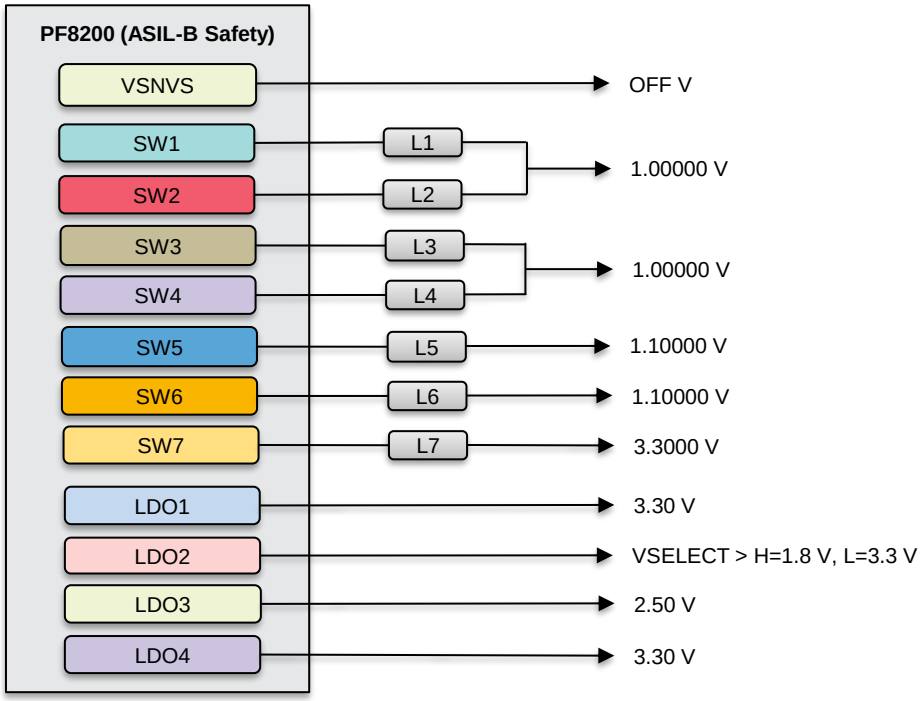
Type number[1]	Package		
	Name	Description	Version
MC33PF8200DBES	WF-Type HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-21 (DD/SC)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power up sequence summary



6 Hardware configuration diagram



7 OTP configuration

See PF8100_PF8200 data sheet for parametric details. The OTP configuration summary for DB (sequence ID) is provided in Table 2, Table 3 and Table 4.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
I^2C settings	Device address	0x09
	I^2C CRC	Enabled
VIN OV lockout	VIN_OVLO	Enabled
	VIN_OVLO shutdown	Disabled
	VIN_OVLO debounce	100 µs
Power good	PG check on power up	RESETBMCU is released regardless of the OV/UV status
	PGOOD pin operation	Power good indicator
	PGOOD pin controlled by	SW1, SW2, SW3, SW4, SW5, SW6, SW7, LDO1, LDO2, LDO3, LDO4
PWRON control	Power on event detection	Level sensitive
	PWRON debounce	32 ms
	TRESET time	2 sec
	TRESET behavior	PMIC shutdown
STANDBY control	STANDBY polarity	STANDBY active high
EWARN timer	EWARN delay	0.1 ms before power down sequence
XFAILB pin	XFAIL operation	XFAILB operation enabled
FSOB control	FSOB operating mode	Fault status mode
	Assertion on hard-fault event	Disabled
	Assertion on WD timer event	Disabled
	Assertion on WDI event	Disabled
	Assertion on soft-fault event	Disabled
WDI control	WDI reset type	Hard WD reset
	WDI polarity	WDI event detected on rising edge
	WDI detection in standby	Disabled
	Regulators affected by WDI event	n/a
Watchdog timer control	WD timer	Disabled at power-up
	WD clear window	100 % window
	WD window duration	1024 ms
	Expire fails before WD event	8
	Maximum WD event counter	16
	WD timer in standby	Disabled
Frequency control	Nominal switching frequency	2.5 MHz
	SYNCOUT operation	Disabled
	SYNCIN operation	Disabled
	Frequency spread spectrum	Disabled
ASILB functional safety	Fail safe state	Disabled
	Max FS counter	16
	FS self-clear timer	60 min
	Bandgap comparator	Shutdown enabled
	Secure write	Disabled

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
Fault management	Fault timer	Disabled
	Maximum fault counter	Disabled
	OV bypass selection	No OV bypass selected
	UV bypass selection	No UV bypass selected
	ILIM bypass selection	SW1, SW2, SW3, SW4, SW5, SW6, SW7, LDO1, LDO2, LDO3, LDO4
Switching mode	Default SW operating mode	PWM

Table 3. Sequencer OTP configuration

Functional block	Feature	OTP selection
Power up sequencing	Sequencer TBASE	250 µs
	SW1 sequence slot	Regulator disabled
	SW2 sequence slot	Regulator disabled
	SW3 sequence slot	Regulator disabled
	SW4 sequence slot	Regulator disabled
	SW5 sequence slot	2
	SW6 sequence slot	5
	SW7 sequence slot	2
	LDO1 sequence slot	Regulator disabled
	LDO2 sequence slot	Regulator disabled
	LDO3 sequence slot	Regulator disabled
	LDO4 sequence slot	Regulator disabled
	RESETBMCU sequence slot	20
	PGOOD sequence slot	PGOOD not set in sequence
Power down sequencing	Power down mode	Mirror power up sequence
	SW1 power down group	Group 4 (1st)
	SW2 power down group	Group 4 (1st)
	SW3 power down group	Group 4 (1st)
	SW4 power down group	Group 4 (1st)
	SW5 power down group	Group 4 (1st)
	SW6 power down group	Group 4 (1st)
	SW7 power down group	Group 4 (1st)
	LDO1 power down group	Group 4 (1st)
	LDO2 power down group	Group 4 (1st)
	LDO3 power down group	Group 4 (1st)
	LDO4 power down group	Group 4 (1st)
	PGOOD power down group	Group 4 (1st)
	RESETBMCU power down group	Group 4 (1st)
	RESETBMCU group delay	10 µs
	Group 1 power down delay	120 µs
	Group 2 power down delay	120 µs
	Group 3 power down delay	120 µs
	Group 4 power down delay	120 µs
	Power down delay	5.0 ms

Table 4. Regulators OTP configuration

Functional block	Feature	OTP selection
SW1 (Dual phase master)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/µs
	Switching phase	0°
	Output inductor	1.0 µH
SW2 (Dual phase slave)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/µs
	Switching phase	225°
	Output inductor	1.0 µH
SW3 (Dual phase slave)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/µs
	Switching phase	0°
	Output inductor	1.0 µH
SW4 (Dual phase master)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/µs
	Switching phase	225°
	Output inductor	1.0 µH
SW5 (Single phase)	Output voltage	1.1 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/µs
	Switching phase	45°
	Output inductor	1.0 µH
SW6 (Single phase)	Output voltage	1.1 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/µs
	Switching phase	270°
	Output inductor	1.0 µH
	VTT mode	Disabled
SW7	Output voltage	3.3 V
	Current limit	2.6 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	Switching phase	180°
	Output inductor	1.0 µH

Table 4. Regulators OTP configuration

Functional block	Feature	OTP selection
LDO1 regulator	Output voltage	3.3 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
LDO2 regulator	Output voltage	3.3 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
	LDO2EN hardware control	Disabled
	VSELECT hardware control	Enabled
LDO3 regulator	Output voltage	2.5 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
LDO4 regulator	Output voltage	3.3 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
VSNVS	Output voltage	OFF V
Coincell	Coin cell voltage	3.0 V

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