Functional Safety Information

LM62440-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the LM62440-Q1 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

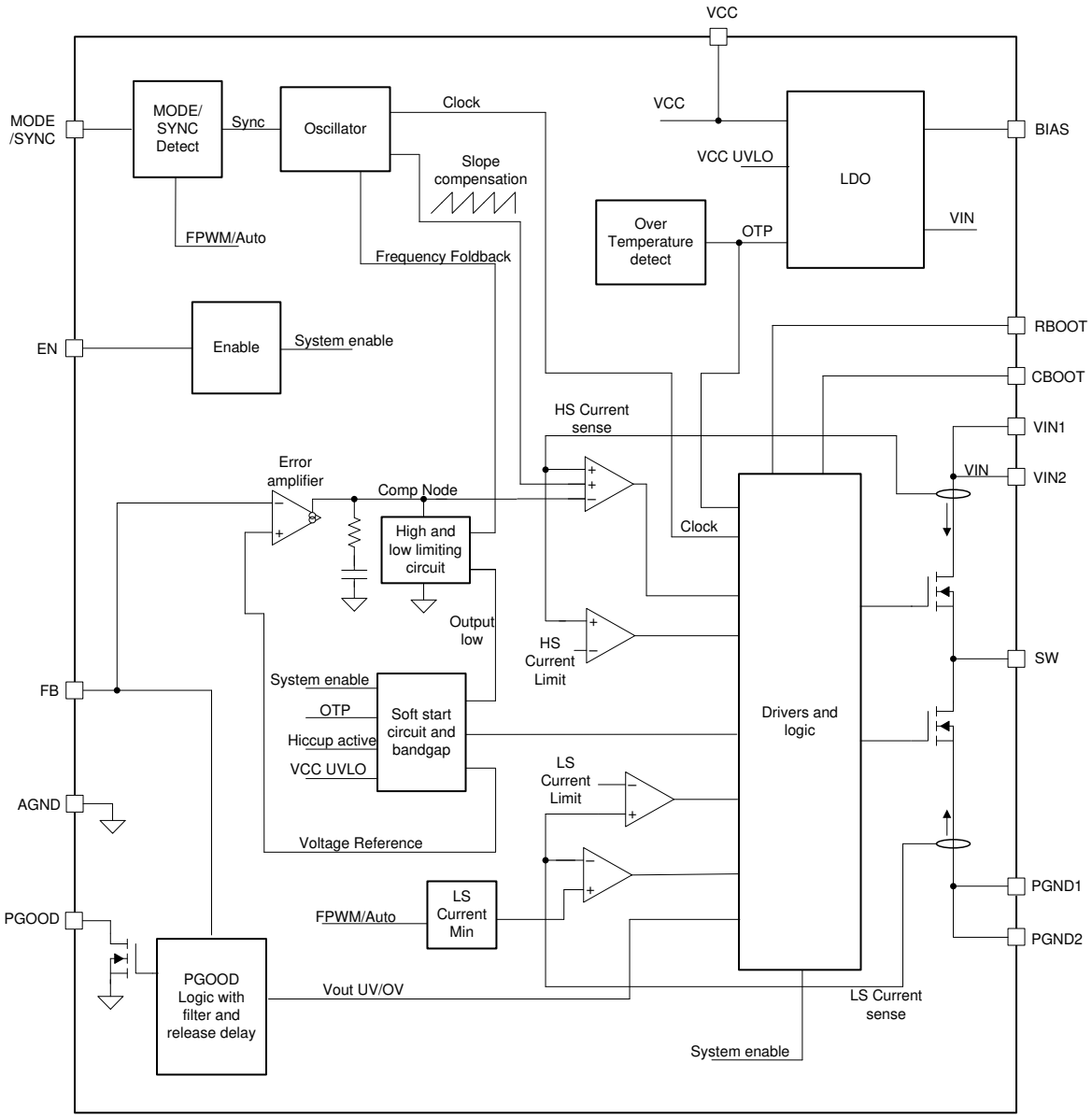

Figure 1-1. Functional Block Diagram

The LM62440-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM62440-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	8
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM62440-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW No output	45
SW output not in specification – voltage or timing	40
SW power FET stuck on	5
PGOOD false trip, fails to trip	5
Short circuit any two pins	5

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM62440-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM62440-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the *LM62440-Q1 Automotive 3-V to 36-V, 4-A, Low-Noise Synchronous Step-Down Converter* data sheet.

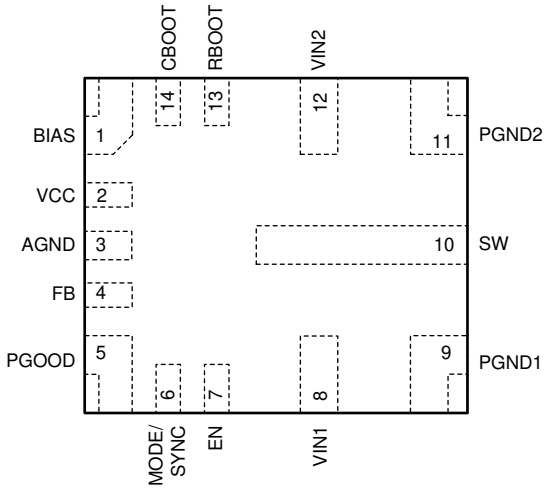

Figure 4-1. Pin Diagram

The following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit, as per the *LM62440-Q1 Automotive 3-V to 36-V, 4-A, Low-Noise Synchronous Step-Down Converter* data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Normal operation if the pin is not tied directly to V_{OUT}. V_{OUT} = 0 V if tied directly to V_{OUT}.	B
VCC	2	V_{OUT} = 0 V	B
AGND	3	Normal operation	D
FB (ADJ option)	4	V_{OUT} >> than programmed output voltage	B
FB (3.3 V or 5 V option)	4	V_{OUT} = 0 V if the pin has no resistor between V_{OUT} and FB. Otherwise, V_{OUT} >> than programmed output voltage.	B
PGOOD	5	PGOOD is not valid signal. V_{OUT} is in regulation.	D

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	6	Auto mode with spread spectrum operation	C
EN	7	V_{OUT} = 0 V	B
VIN1	8	V_{OUT} = 0 V	B
PGND1	9	Normal operation	D
SW	10	Damage to the HS FET	A
PGND2	11	Normal operation	D
VIN2	12	V_{OUT} = 0 V	B
RBOOT	13	V_{OUT} = 0 V	A
CBOOT	14	V_{OUT} = 0 V	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Normal operation	D
VCC	2	VCC output is unstable and can increase above 5.5-V rating of the VCC pin.	A
AGND	3	V_{OUT} can be abnormal due to switching noise on analog circuits.	B
FB	4	V_{OUT} >> than programmed output voltage	B
PGOOD	5	PGOOD not valid signal. V_{OUT} is in regulation.	D
MODE/SYNC	6	Auto mode versus FPWM operation and spread spectrum cannot be predicted.	C
EN	7	Unpredictable operation	B
VIN1	8	V_{OUT} is normal. Current loop is affected, potentially affecting noise, jitter, EMI, and reliability.	C
PGND1	9	V_{OUT} is normal. Current loop is affected, potentially affecting noise, jitter, EMI, and reliability.	C
SW	10	V_{OUT} = 0 V	B
PGND2	11	V_{OUT} is normal. Current loop is affected, potentially affecting noise, jitter, EMI, and reliability.	C
VIN2	12	V_{OUT} is normal. Current loop is affected, potentially affecting noise, jitter, EMI, and reliability.	C
RBOOT	13	V_{OUT} normal, low efficiency	C
CBOOT	14	V_{OUT} = 0 V	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	VCC	VCC ESD clamp is damaged if BIAS > 5.5 V.	A
VCC	2	AGND	V_{OUT} = 0 V	B
AGND (ADJ option)	3	FB	V_{OUT} >> than programmed output voltage	B
AGND (3.3 V or 5 V option)	4	FB	V_{OUT} = 0 V if there is no resistor between V_{OUT} and FB. Otherwise, V_{OUT} >> than the programmed output voltage.	B
FB (ADJ option)	4	PGOOD	V_{OUT} = 0 V. Damage if PGOOD > 16 V	A
FB ((3.3 V or 5 V option)	4	PGOOD	V_{OUT} is normal. PGOOD is damaged if there is no resistor between FB and VOUT. V_{OUT} = 0 V, otherwise, damage if PGOOD > 16 V.	A
PGOOD	5	MODE/SYNC	V_{OUT} normal. The device operates in auto mode with spread spectrum after start-up.	D
MODE/SYNC	6	EN	V_{OUT} normal, the devices operates in FPWM mode with no spread spectrum.	D
EN	7	VIN1	Normal operation	D
VIN1	8	PGND1	V_{OUT} = 0 V. Damage to low-side circuitry if PGND >> AGND	B
PGND1	9	SW	Damage to the HS FET	A
SW	10	PGND2	Damage to the HS FET	A

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND2	11	VIN2	V_{OUT} = 0 V. Damage to low-side circuitry if PGND >> AGND	B
VIN2	12	RBOOT	V_{OUT} = 0 V. RBOOT ESD clamp runs current to destruction.	A
RBOOT	13	CBOOT	V_{OUT} is normal.	D
CBOOT	14	BIAS	V_{OUT} = 0 V	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	If VIN exceeds 16 V, damage occurs. If VIN is below 16 V, normal operation	A
VCC	2	If VIN exceeds 5.5 V, damage occurs.	A
AGND	3	V_{OUT} = 0 V. Damage to other pins referred to GND	A
FB	4	If VIN exceeds 16 V, damage occurs. V_{OUT} = 0 V	A
PGOOD	5	V_{OUT} = 0 V. PGOOD ESD clamp runs current to destruction.	A
MODE/SYNC	6	V_{OUT} is normal. The part runs in FPWM mode without spread spectrum.	D
EN	7	V_{OUT} is normal.	D
VIN1	8	Normal operation	D
PGND1	9	V_{OUT} = 0 V. Damage to low-side circuitry if PGND >> AGND	B
SW	10	Damage to the LS FET	A
PGND2	11	V_{OUT} = 0 V. Damage to low-side circuitry if PGND >> AGND	B
VIN2	12	Normal operation	D
RBOOT	13	V_{OUT} = 0 V. RBOOT ESD clamp runs current to destruction.	A
CBOOT	14	V_{OUT} = 0 V. CBOOT ESD clamp runs current to destruction.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2020) to Revision A (May 2022) **Page**

- Updated to new pin FMA template and added pin FMA information..... 5

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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