Application Report
SNVA798–December 2017

Designing a Feedforward Capacitor for LMR140x0

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ABSTRACT

The feedforward capacitor is a capacitor placed across the high-side feedback resistor to improve loop stability and transient performance. The LMR14020/30/50 devices are a family of wide V_{IN}, internally compensated, peak-current mode buck converters. This application report analyzes the impact of the feedforward capacitor value on key parameters of the loop response such as bandwidth, phase margin, and gain margin. The application report also provides the methods to design a feedforward capacitor.

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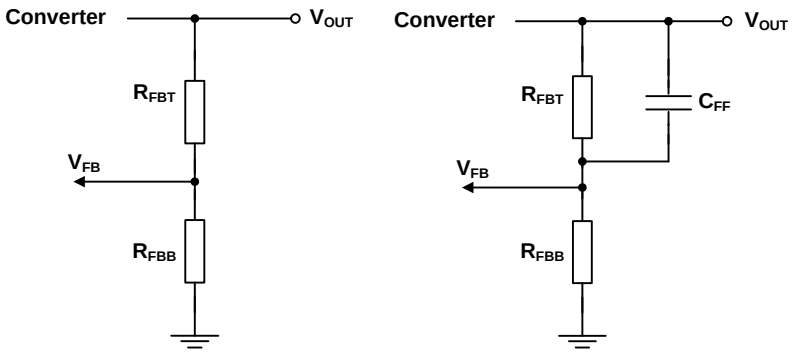
Trademarks

1 Loop Response With Feedforward Capacitor

The LMR140x0 family of devices are peak-current mode buck converters. They have internal loop compensation with the operational transconductance amplifier. The standard feedback network consists of two resistors used to set the output voltage of the converter, as shown in Figure 1. A common method to improve the stability and bandwidth of the converter is to place an additional capacitor (C_{FF}) in parallel with the high-side feedback resistor (R_{FBT}), see Figure 1.



(a) Standard feedback network (b) Feedback network with feedforward capacitor

Figure 1. Feedback Network With and Without Feedforward Capacitor

For both configurations, the output voltage is set by the two feedback resistors, see Equation 1.

$$\frac{V_{OUT}}{V_{REF}} = \frac{R_{FBB} + R_{FBT}}{R_{FBB}} \tag{1}$$

Equation 2 shows the transfer function for the standard feedback network.

$$G1(s) = \frac{v_{FB}}{v_{OUT}} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}} \tag{2}$$

Equation 3 shows the transfer function for the feedback network with the feedforward capacitor.

$$G2(s) = \frac{v_{FB}}{v_{OUT}} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}} \times \frac{1 + s \times R_{FBT} \times C_{FF}}{1 + s \times (R_{FBT} \,//\, R_{FBB}) \times C_{FF}} \tag{3}$$

The feedback network is part of the loop of the converter. By comparing Equation 2 and Equation 3, we can see that the impact of the feedforward capacitor to the new loop (G_{Loop_new}), is that it brings an additional transfer function (G_{Cff}) to the original loop ($G_{Loop\_original}$), see Equation 4 and Equation 5.

$$G_{Loop\_new}(s) = G_{Loop\_original}(s) \times G_{Cff}(s) \tag{4}$$

$$G_{Cff}(s) = \frac{1 + s \times R_{FBT} \times C_{FF}}{1 + s \times (R_{FBT} \,//\, R_{FBB}) \times C_{FF}} \tag{5}$$

Substitute Equation 1 into Equation 5 to get Equation 6.

$$G_{Cff} = \frac{1 + \frac{s}{2\pi} \times \frac{1}{f_0 \times \sqrt{\frac{V_{REF}}{V_{OUT}}}}}{1 + \frac{s}{2\pi} \times \frac{1}{f_0 \times \sqrt{\frac{V_{OUT}}{V_{REF}}}}} = \frac{1 + j\frac{f}{f_0} \times \sqrt{\frac{V_{OUT}}{V_{REF}}}}{1 + j\frac{f}{f_0} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{6}$$

With Equation 7:

$$f_0 = \frac{1}{2\pi \times R_{FBT} \times C_{FF}} \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \quad (7)$$

From Equation 6, we know that the feedforward capacitor introduces one zero and one pole to the original loop, see Equation 8 and Equation 9.

$$f_Z = f_0 \times \sqrt{\frac{V_{REF}}{V_{OUT}}} \quad (8)$$

$$f_P = f_0 \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \quad (9)$$

2 Feedforward Capacitor Design Based on the LMR14020

2.1 Original Loop and Design Target

Figure 2 and Figure 3 show the original schematic and loop response without the feedforward capacitor. The loop response is measured under f_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 3.3 V, and I_{OUT} = 2 A. The high-side feedback resistor, R_{FBT} = 56.2 kΩ. The transient response is better with higher bandwidth. It is suggested that the bandwidth should be limited to 1/5 of the switching frequency. In this application, the phase margin design target is larger than 50° and the gain margin design target is larger than 10 dB. C_{FF} is required to improve the phase margin and gain margin, as well as to increase bandwidth to the desired value.

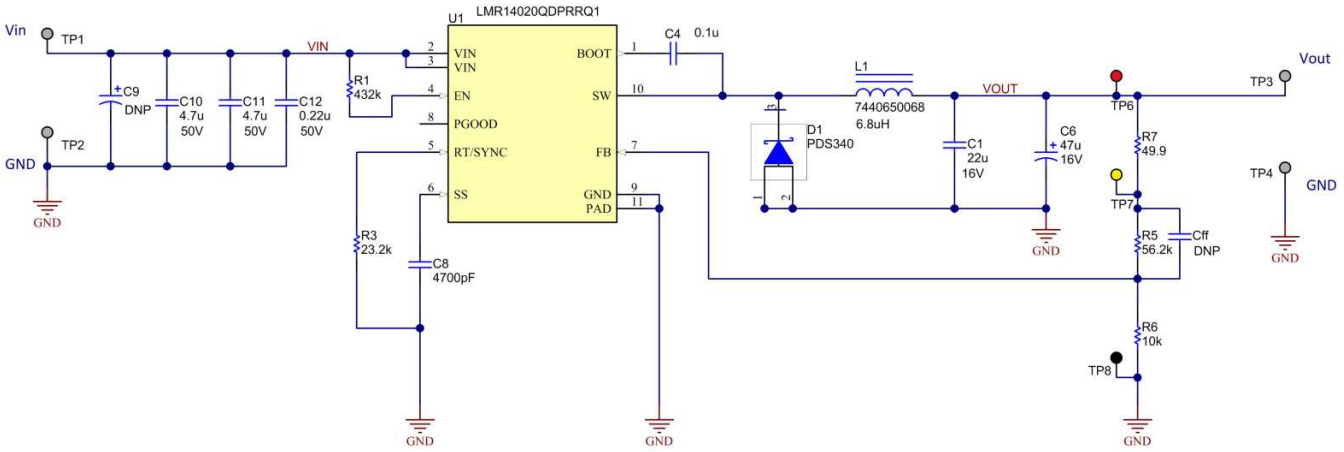


Figure 2. Original Schematic Without Feedforward Capacitor

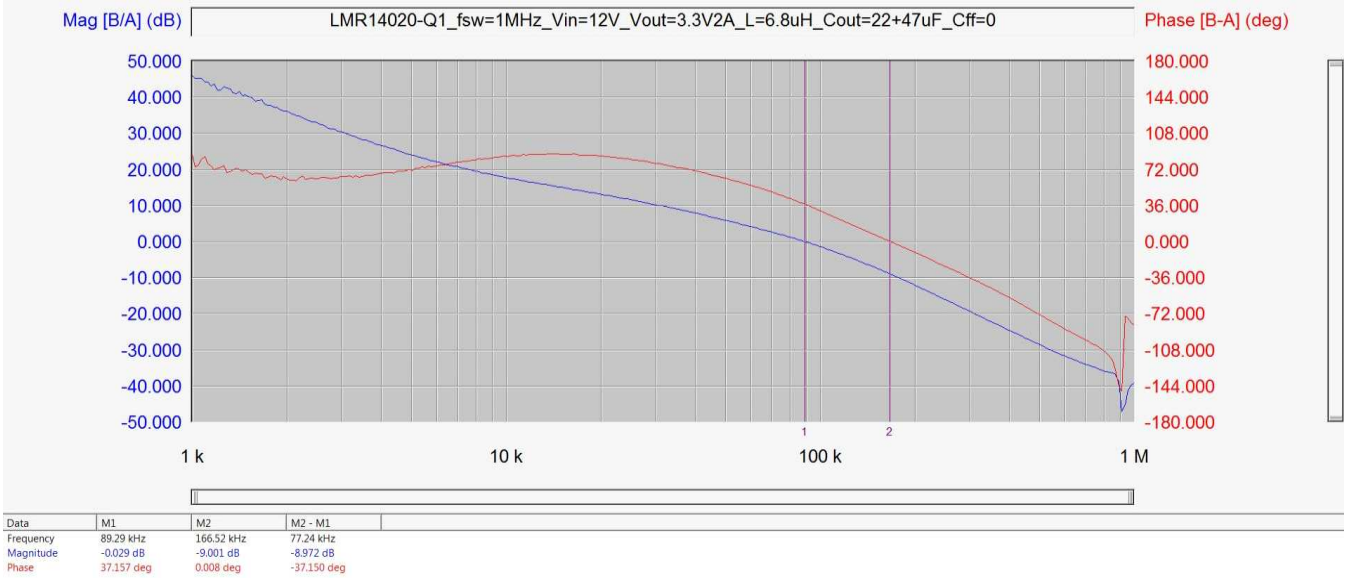


Figure 3. Original Loop Response Without Feedforward Capacitor

Table 1 lists the original loop performance and design target.

Table 1. Original Loop Performance and Design Target

Loop Response Item	Original Loop	Design Target
Bandwidth	89 kHz	≤ 200 kHz
Phase margin	37°	> 50°
Gain margin	9 dB	> 10 dB

2.2 Additional Transfer Function Introduced by the Feedforward Capacitor

The reference voltage, V_{REF}, of the LMR14020 device is 0.75 V and V_{OUT} = 3.3 V in this application. Based on Equation 6 to Equation 9, when C_{FF} = 10 pF and C_{FF} = 100 pF, the bode plot of G_{Cff} is plotted as shown in Figure 4 and Figure 5. The feedforward capacitor value, C_{FF}, only determines f_0 if C_{FF} increases, then f_0 decreases, and the curve of G_{Cff} shifts left. The shape of G_{Cff} remains unchanged with a different C_{FF}.

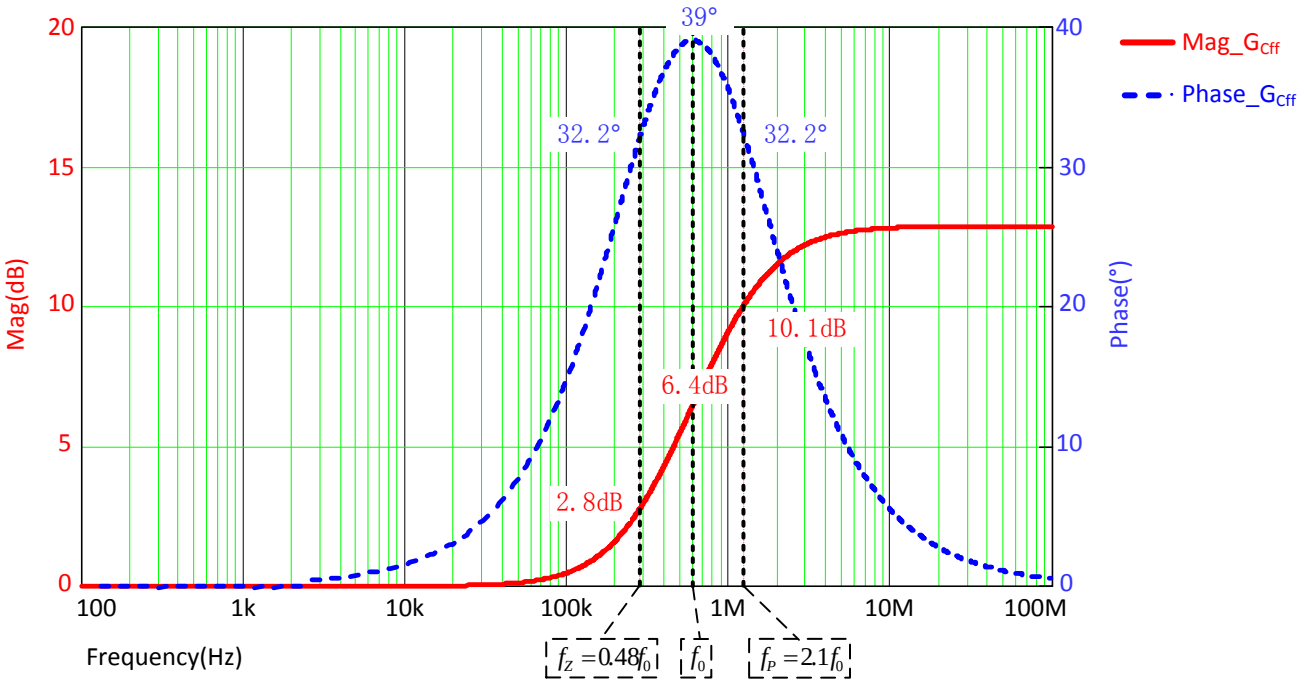


Figure 4. Bode Plot of Additional Transfer Function G_{Cff} When C_{FF} = 10 pF

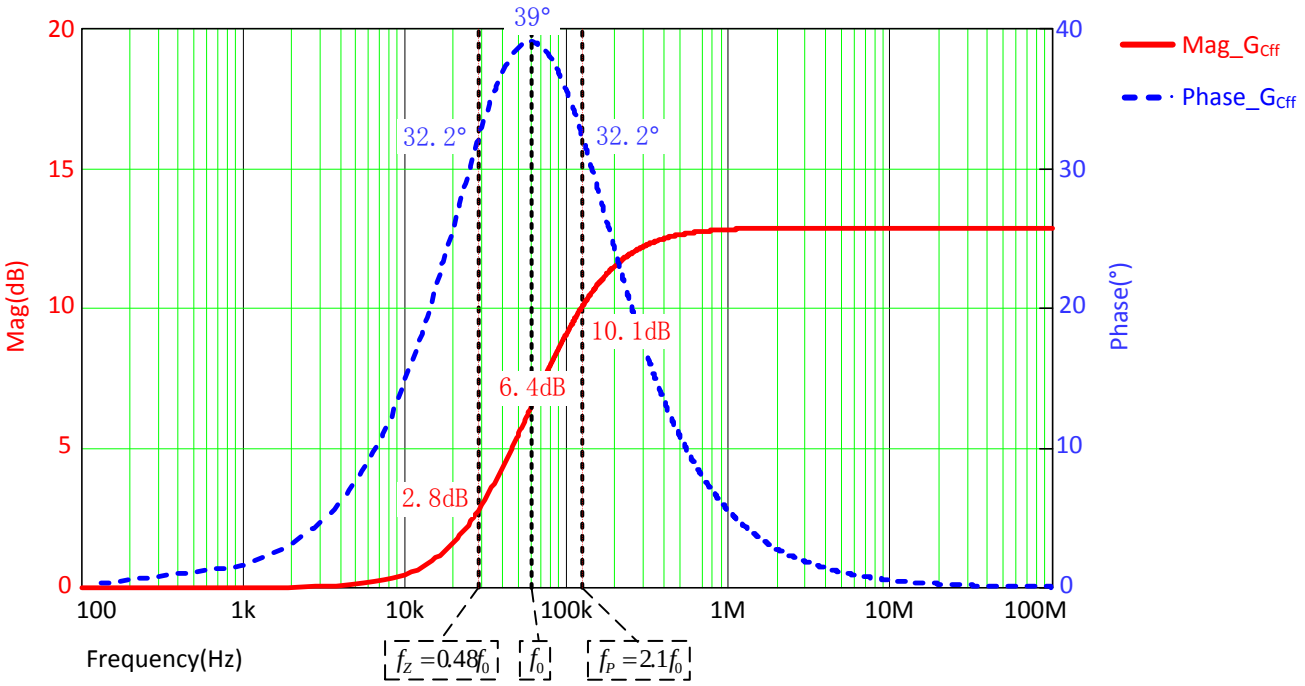


Figure 5. Bode Plot of Additional Transfer Function G_{Cff} When C_{FF} = 100 pF

2.3 Bandwidth and Feedforward Capacitor Value Limit

From Figure 4, the magnitude of G_{Cff} is positive, which makes the loop gain positive at the original crossover frequency. The new crossover frequency, f_{C_new}, is higher and the loop bandwidth is increased by the feedforward capacitor.

The target bandwidth limitation is set to 200 kHz. From Figure 3, the magnitude of the original loop is –12 dB at 200 kHz. G_{Cff} must provide 12-dB magnitude at 200 kHz to make the new loop gain 0 dB at 200 kHz. In Equation 6 and Equation 7, f = 200 kHz, $20\log|G_{Cff}|$ = 12 dB, and R_{FBT}= 56.2 kΩ, so solve the equation to get f_0= 46.6 kHz, C_{FF}= 127 pF.

If C_{FF} increases, the curve of G_{Cff} shifts left. The magnitude of G_{Cff} is larger at the original crossover frequency, and this makes the new bandwidth larger. Therefore, the larger the feedforward capacitor value, the higher the bandwidth. To ensure bandwidth ≤ 200 kHz, a C_{FF} ≤ 127 pF must be designed.

2.4 Phase Margin and Feedforward Capacitor Value Limit

As described in Section 2.3, to satisfy the bandwidth design target, a C_{FF} ≤ 127 pF must be designed. With a larger C_{FF}, the bandwidth is higher, and the transient response is better. Check C_{FF} = 100 pF first.

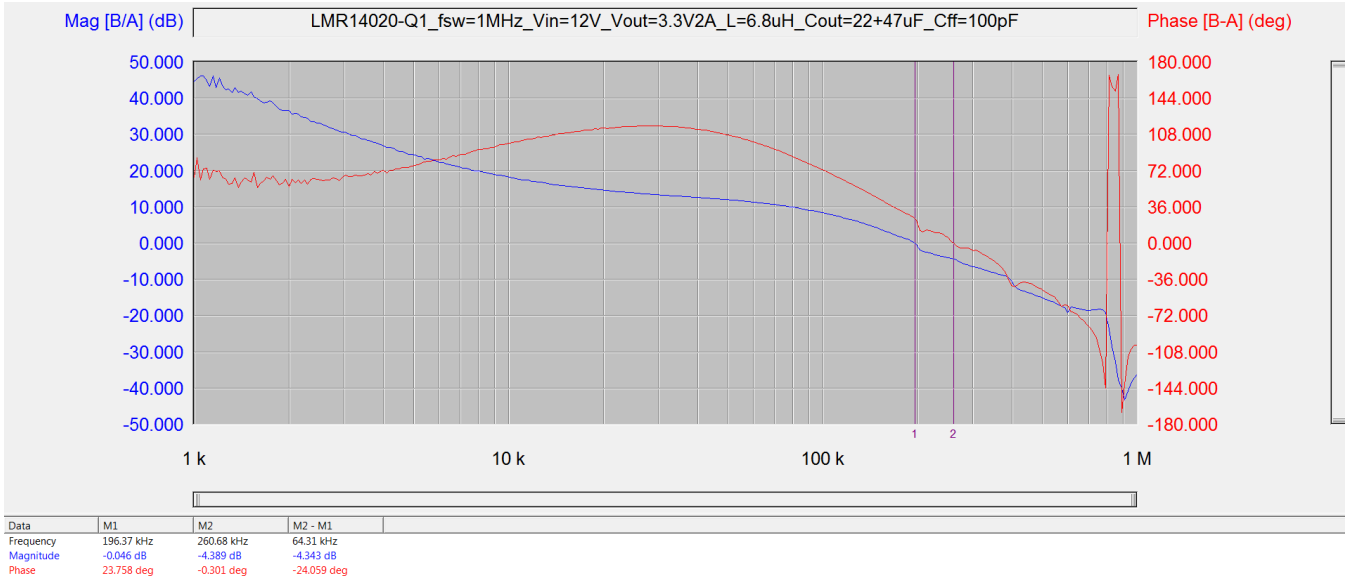


Figure 6. Loop Response With 100-pF Feedforward Capacitor

The loop response with C_{FF} = 100 pF is measured as shown in Figure 6. Phase margin is 23.8°, which is smaller than the design target. Here, f_C is defined as the cross over frequency, and f_C = 196 kHz with C_{FF} = 100 pF. From Equation 7, f_0 = 59 kHz and $f_0 < f_C$. To get a higher phase margin, check C_{FF} = 47 pF.

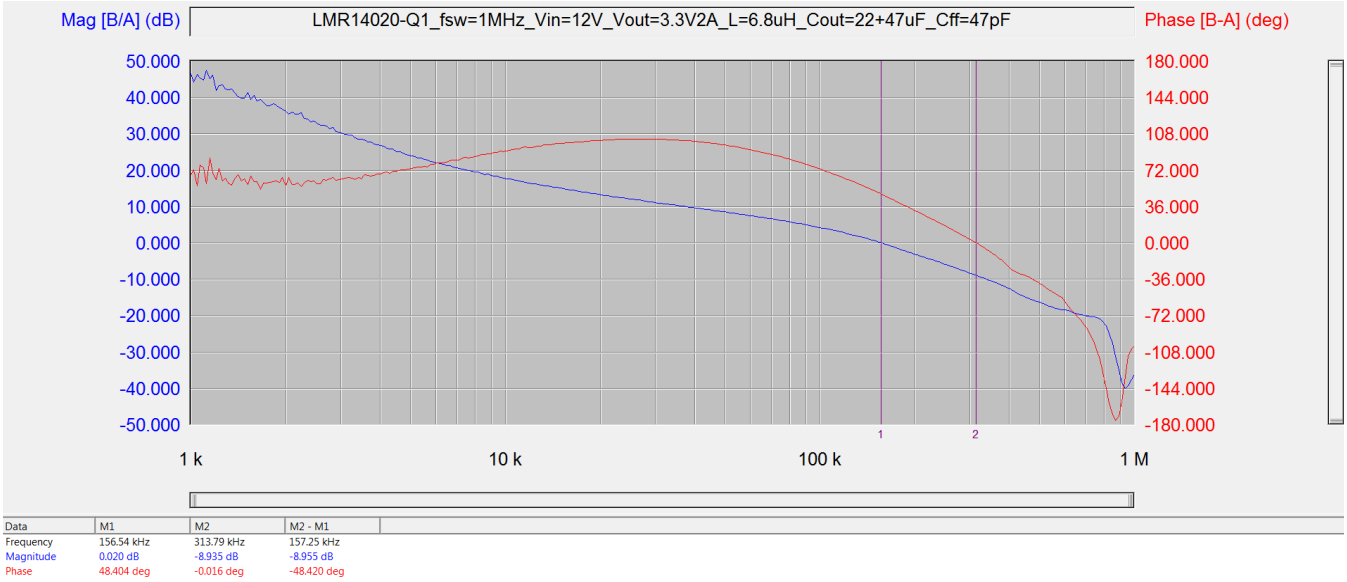


Figure 7. Loop Response With 47-pF Feedforward Capacitor

The loop response with C_{FF} = 47 pF is measured as shown in Figure 7. Phase margin is 48.4°, which is smaller than the design target. Here f_C = 157 kHz. From Equation 7, f_0 = 126 kHz and $f_0 < f_C$.

Now, let us consider how phase margin changes with a larger C_{FF} value, $C_{FF\_new} > 47$ pF. After adding the feedforward capacitor, the phase of G_{Cff} is added to the original loop. The phase margin for C_{FF} = 47 pF and C_{FF_new} are as follows in Equation 10 and Equation 11.

$$\text{PhaseMargin}_{47pF} = \text{Phase}_{\text{OriginalLoop}}@f_{C\_47pF} + \text{Phase}_{G_{Cff}\_47pF}@f_{C\_47pF} \quad (10)$$

$$\text{PhaseMargin}_{new} = \text{Phase}_{\text{OriginalLoop}}@f_{C\_new} + \text{Phase}_{G_{Cff}\_new}@f_{C\_new} \quad (11)$$

The larger the feedforward capacitor value, the higher the bandwidth, so $f_{C\_new} > f_{C\_47pF}$. With a larger C_{FF}, f_0 decreases, and the phase curve of G_{Cff} shifts left. As shown in Figure 8, with a larger C_{FF}, $\text{Phase}_{Gcff\_new}@f_{C\_new} < \text{Phase}_{Gcff\_47pF}@f_{C\_47pF}$.

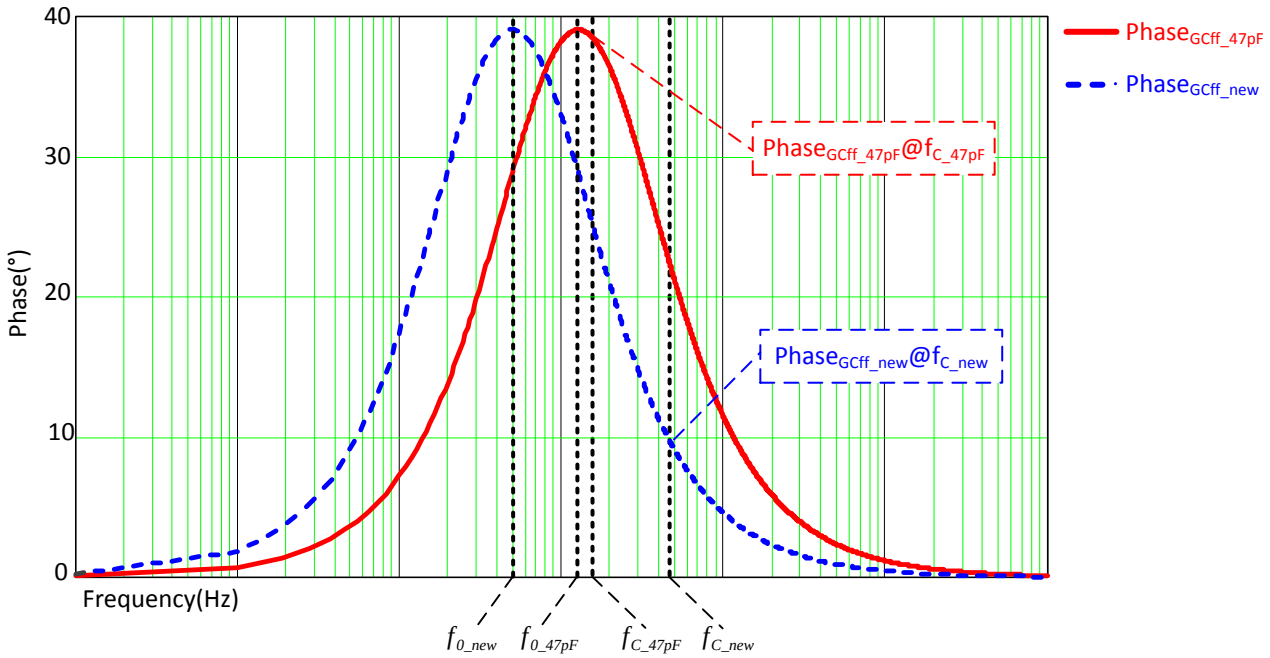


Figure 8. Phase of G_{Cff} When C_{FF} = 47 pF and Larger

As Figure 3 shows, because $f_{C\_new} > f_{C\_47pF}$, the original loop phase is smaller at f_{C_new} than the original loop phase at f_{C_47pF}: $Phase_{OriginalLoop}@f_{C\_new} < Phase_{OriginalLoop}@f_{C\_47pF}$. Considering $Phase_{Gcff\_new}@f_{C\_new} < Phase_{Gcff\_47pF}@f_{C\_47pF}$, Equation 10 and Equation 11, we get the result: $PhaseMargin_{new} < PhaseMargin_{47pF}$. Phase margin is smaller than 48.4° with $C_{FF} > 47$ pF. A slightly smaller C_{FF} is needed to get a 50° phase margin. Check $C_{FF} = 33$ pF.

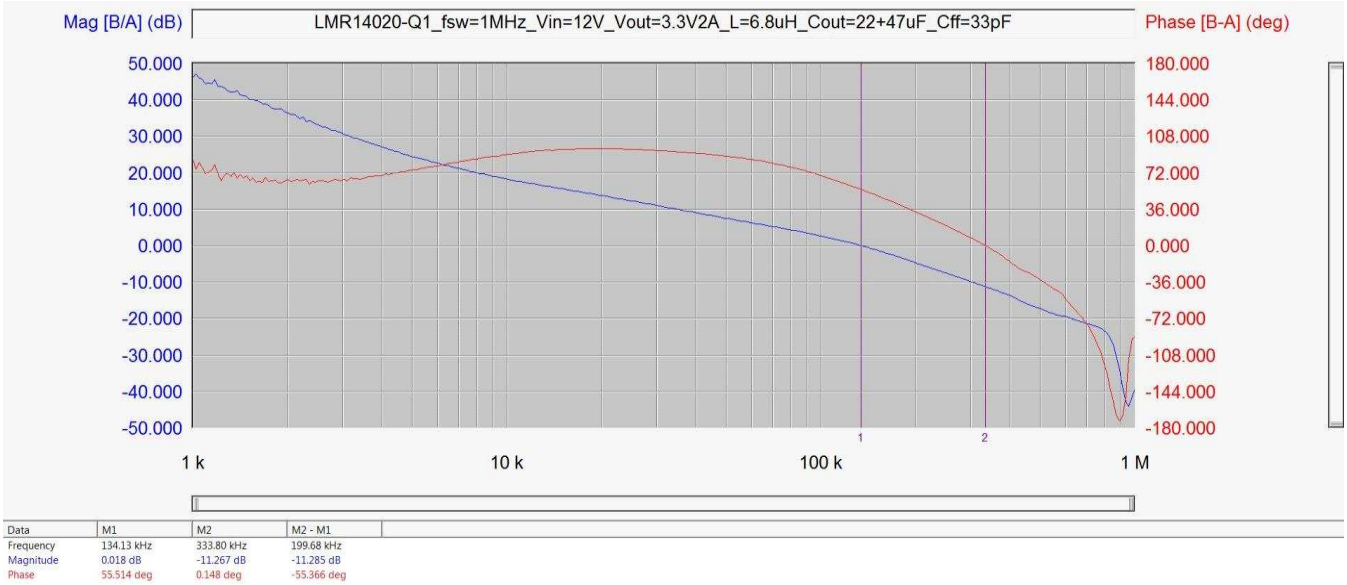


Figure 9. Loop Response With 33-pF Feedforward Capacitor

The loop response with $C_{FF} = 33$ pF is measured as shown in Figure 9. The bandwidth is 134 kHz, phase margin is 55.5°, and gain margin is 11 dB, which satisfies the design target. So $C_{FF} = 33$ pF is at last chosen.

3 Conclusion

The feedforward capacitor brings an additional transfer function, G_{Cff}, to the original loop. The value of the feedforward capacitor determines the horizontal position of G_{Cff}, while the shape of G_{Cff} is determined by V_{OUT} and V_{REF}, which are usually fixed in a specific application. The feedforward capacitor value limit can be obtained based on the bandwidth, phase margin, and gain margin of the design target. In this application report, the process of the feedforward capacitor design is introduced, and the experiment results are provided to verify the theory.

4 References

- Texas Instruments, LMR14020-Q1 SIMPLE SWITCHER 40 V, 2 A Step-Down Converter with 40 μA IQ, data sheet
- Texas Instruments, LMR14020QDPREVM User's Guide
- Texas Instruments, Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor, application report

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