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Evaluating the AD1955 High Performance, Multibit Sigma-Delta DAC with SACD Playback

EVAL-AD1955EBZ PACKAGE CONTENTS

AD1955 evaluation board
USBi control interface board
USB cable

OTHER SUPPORTING DOCUMENTATION

AD1955 data sheet

EVALUATION BOARD OVERVIEW

This document explains the design and setup of the evaluation board for the AD1955. The evaluation board must be connected to an external ±12 V dc power supply and ground. On-board regulators derive 5 V and 3.3 V supplies for the AD1955 and peripherals. The AD1955 is controlled through an SPI interface. A small external interface board, EVAL-ADUSB2EBZ (also called USBi), connects to a PC USB port and provides SPI access to the evaluation board through a ribbon cable. A graphical user interface (GUI) program is provided for easy programming of the chip in a Microsoft® Windows® PC environment. The evaluation board allows demonstration and performance testing of most AD1955 features, including high performance stereo DAC operation.

Additional analog circuitry (DAC I/V converter/filter/buffer) and digital interfaces such as S/PDIF are provided to ease product evaluation.

The board has an S/PDIF receiver with XLR, RCA, and optical connectors, as well as a discrete serial audio interface. Analog interfaces are accessible with XLR or RCA connectors.

FUNCTIONAL BLOCK DIAGRAM

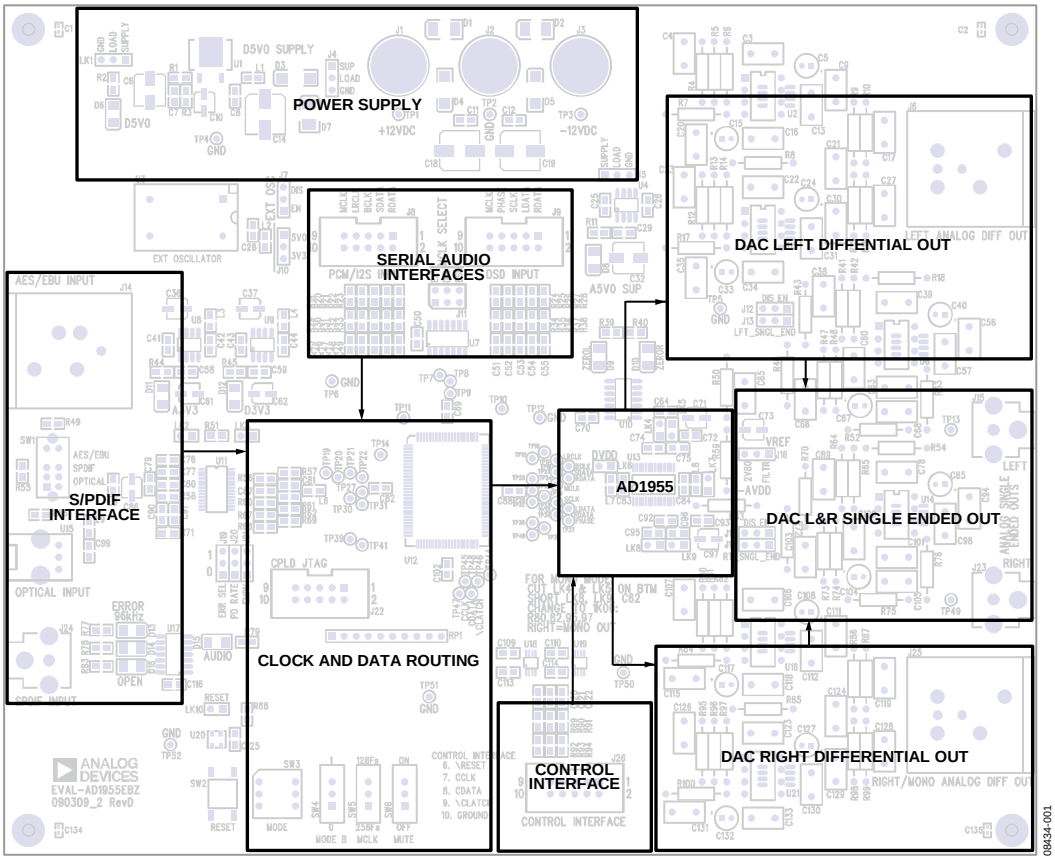

Figure 1.

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REVISION HISTORY

2/10—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

STANDALONE MODE

By default, with no control interface connected, the evaluation board and AD1955 DAC run in standalone mode, which fixes the functionality of the AD1955 into I²S data format, running at 256 × f_S (default register condition). The default configuration of the evaluation board routes clock and audio data from the selected S/PDIF input through the CPLD and to the AD1955 DAC. Other serial audio routing configurations are described in the Digital Audio Connections and Routing section.

SPI CONTROL

The evaluation board can be configured for live control over the registers in the AD1955. When the **Automated Register Window Builder** software is installed and the USBi control interface is plugged into the board, the software controls the AD1955. The **Automated Register Window Builder** is available for download at http://www.analog.com/AD1955.

AUTOMATED REGISTER WINDOW BUILDER SOFTWARE INSTALLATION

The **Automated Register Window Builder** is a program that launches a graphical user interface for direct, live control of the AD1955 registers. The GUI content for the part is defined in a part-specific .xml file; this file is included in the software installation. To install the **Automated Register Window Builder** software, follow these steps:

1. At **www.analog.com/AD1955**, find the **Resources & Tools** list.
2. In the list, find **Evaluation Boards & Development Kits** and click **Evaluation Boards/Tools** to open the provided **ARWBvXX.zip** file.
3. Double-click the provided **.msi** file to extract the files to an empty folder on your PC.
4. Then double-click **setup.exe** and follow the prompts to install the **Automated Register Window Builder**. A computer restart is not required.
5. Copy the .xml file for the AD1955 from the extraction folder into the **C:\Program Files\Analog Devices Inc\AutomatedRegWin** folder, if it does not appear in the folder after installation.

HARDWARE SETUP—USBi

To set up the USBi hardware, follow these steps:

1. Plug the USBi ribbon cable into the J26 control interface header.
2. Connect the USB cable to your computer and to the USBi.
3. When prompted for drivers, follow these steps:
   a. Choose **Install from a list or a specific location**.
   b. Choose **Search for the best driver in these locations**.
   c. Check the box for **Include this location in the search**.
   d. Find the USBi driver, **C:\Program Files\ Analog Devices Inc\AutomatedRegWin\USB drivers**.
   e. Click **Next**.
   f. If prompted to choose a driver, select **CyUSB.sys**.
   g. If the PC is running Windows XP and a message appears saying that the software has not passed Windows logo testing, click **Continue Anyway**.

You can now open the **Automated Register Window Builder** application and load the .xml file for the part on your evaluation board.

POWERING THE BOARD

The AD1955 evaluation board requires a power supply input of ±12 V dc and ground to the three binding posts; +12 V draws ~250 mA and −12 V draws ~100 mA. The on-board regulators provide two 3.3 V and two 5.0 V rails. The 3.3 V rails supply AVDD and DVDD for the active peripheral components on the board. The 5.0 V rails provide voltage to both the peripherals and the AD1955. D5V0 (see Figure 3) provides power for the CPLD routing IC, as well as power for DVDD of the AD1955. A5V0 (see Figure 4) provides power only for AVDD of the AD1955.

Links are provided along the power rails to give access for current measurement. These links also allow the user to supply voltage from an outside source. All of these links are hardwired by a trace on the backside of the PCB.

The 3.3 V rails, A3V3 and D3V3, each have a link, LK2 and LK3, that can isolate the S/PDIF receiver. The links are shown in Figure 2.

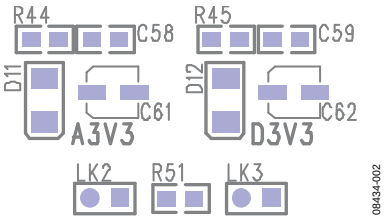

Figure 2. A3V3 and D3V3 Rail Links

The D5V0 supply has two links; J4 is before the on-board regulator and LK1 is after. LK1 provides power for the AD1955, as well as the other 5V0 peripherals. These links are shown in Figure 3.

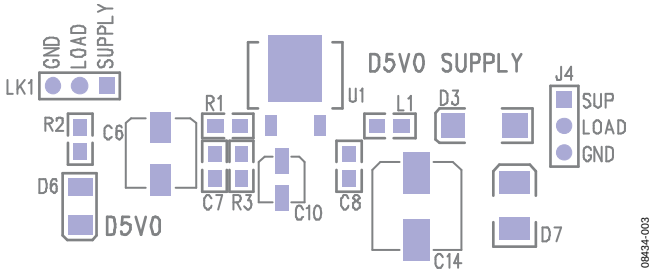

Figure 3. D5V0 Rail Links

The A5V0 link, J5, is before the regulator shown in Figure 4.

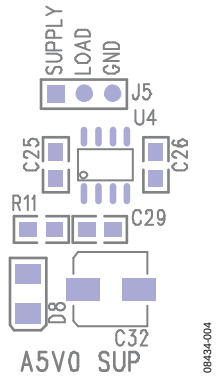

Figure 4. A5V0 Rail Link, Preregulator

Additionally, the AD1955 has local power links for both AVDD and DVDD, as shown in Figure 5. The only components on the load side of these links are the ferrite bead, the decoupling capacitor, and the AD1955 power pin. These are appropriate places to measure the current drawn by the AD1955.

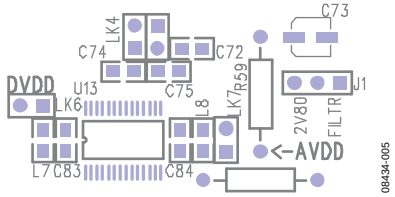

Figure 5. AVDD and DVDD Links for the AD1955

The board has a socket for an active oscillator, U3. Its use is described in the Setting Up the Master Clock (MCLK) section. A jumper is provided to select between 5V0 and 3V3 power, as shown in Figure 6.

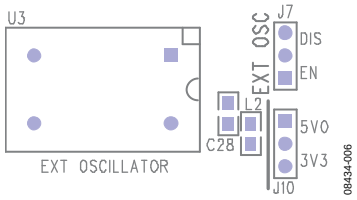

Figure 6. Active Oscillator Power and Enable Jumpers

RESET AND MUTE FOR THE EVALUATION BOARD

The SW2 reset switch on the evaluation board resets three devices: the S/PDIF receiver, the CPLD, and the AD1955. The reset line is held high by a pull-up resistor until the reset switch pulls the line to ground, as shown in Figure 22.

The SW6 mute switch is tied directly to the mute port (Pin 22) of the AD1955.

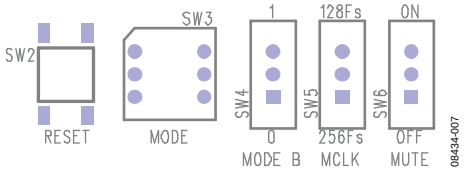

Figure 7. Reset SW2, Mode SW3, and Mute SW6 Switches

SETTING UP THE MASTER CLOCK (MCLK)

The MCLK routing on the evaluation board is normally controlled by the CPLD. The various MCLK sources on the board do not pass through the CPLD; instead, they pass through a series of three-state buffers that are controlled by the CPLD. MCLK can be sourced from the S/PDIF receiver or either of the serial audio headers. The SW3 rotary octal switch, shown in Figure 7, selects the MCLK source, as well as other routing and control options.

There are two features of the board that are not implemented in the CPLD code: the U3 EXT oscillator and the J11 MCLK select jumper block. The EXT oscillator output, shown in Figure 6, drives the OMCK input of the S/PDIF receiver, as well as an unused port on the CPLD. The feed of a clock to the OMCK input of the S/PDIF receiver has the effect of maintaining clock stability and silence from the receiver if the S/PDIF cable is unplugged. The feed to the unused port of the CPLD allows the EXT oscillator to provide MCLK for the entire board.

The J11 MCLK select jumper block allows for hardwiring of the three MCLK sources, providing a direct connection without a buffer in the path. Both of these features can be implemented or modified by changing the CPLD code, which is presented in the CPLD Code section.

Figure 8. MCLK Select Jumper Block J11

DIGITAL AUDIO CONNECTIONS AND ROUTING

The AD1955 evaluation board has three separate inputs for digital audio signals: S/PDIF (labeled DIR on the board), PCM/I2S (labeled EXT), and DSD.

The S/PDIF receiver can handle any of three options: AES/EBU uses the XLR-F jack, J14; S/PDIF uses the RCA jack, J24; and optical uses the Toslink jack, J15. The input is selected using SW1, as shown in Figure 9. Note that the S/PDIF receiver cannot handle a digital waveform at its input of greater than 1 V p-p. Higher amplitude signals cause an apparent decrease in SNR of the AD1955. This issue can be avoided by lowering the amplitude below 1 V p-p; testing has shown that an amplitude of 500 mV p-p works very well. This adjustment is usually available for either the XLR or RCA input in the signal generator.

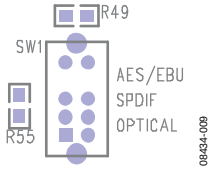

Figure 9. S/PDIF Input Selector Switch SW1

The S/PDIF receiver runs in default mode at 48 kHz and 96 kHz, 256 × f_S. To drive the receiver with 192 kHz, the rate must be changed to 128 × f_S. Figure 7 shows the SW5 MCLK switch, which selects the S/PDIF receiver MCLK mode. After setting

SW5 to the desired f_S rate, the board must be reset using SW2. Next, the AD1955 sample rate register must be set using the **Automated Register Window Builder**. DAC Control Register 0 [9:8] must be set to 10.

The PCM/I2S and DSD headers shown in Figure 10 offer ways of feeding serial digital audio into the AD1955. The serial audio connectors use 1 × 2 100 mil spaced headers, signal, and ground. The odd numbered pins are the ground connections.

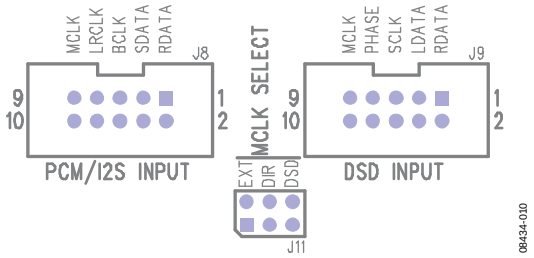

Figure 10. PCM/I2S and DSD Headers

Routing of the BCLK, LRCLK, and SDATA signals is handled by the CPLD, controlled by the SW3 rotary mode select switch shown in Figure 7. Table 1 details the available selections.

Table 1. SW3 Rotary Mode Select

Position	Function
0	S/PDIF input, I²S format, 48 kHz – 96 kHz fs
1	S/PDIF input, left justified, 48 kHz – 96 kHz fs
2	S/PDIF input, DSP format, 48 kHz – 96 kHz fs
3	S/PDIF input, 24-bit right justified, 48 kHz – 96 kHz fs
4	S/PDIF input, 16-bit right justified, 48 kHz – 96 kHz fs
5	PCM/I²S input (J8)
6	DSD input (J9)
7	S/PDIF input, I²S format, 192 kHz fs

VREF JUMPER

The current-to-voltage (I-to-V) converters are biased on the non-inverting inputs of the summing amps. A jumper is provided to select between two settings. The 2v80 reference is derived from a filtered voltage divider; this selection provides the best performance from the circuit (see Figure 11).

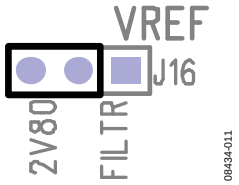

Figure 11. 2V80 Selected as VREF

Alternatively, there is an option to use the FILTR reference of the AD1955 as the VREF for the I-to-V converter. This selection offers better stability over a wide temperature range at the cost of slightly reduced performance (see Figure 12).

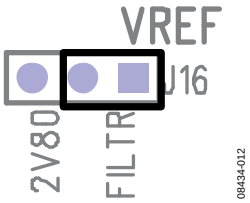

Figure 12. FILTR Selected as VREF

It is also be possible to supply an external VREF by connecting the voltage source directly to the center pin of J16.

CONNECTING ANALOG AUDIO CABLES

There are two forms of the analog outputs of the AD1955 evaluation board: differential and single ended. The differential outputs use XLR-M jacks, following the standard Pin 2 hot, and have a maximum differential output level of 6 V rms when the DAC is fed with a 0 dBFS signal. The single-ended outputs use RCA jacks and have a maximum output level of 2 V rms.

The extra load of the difference amplifier on the I-to-V converter increases the THD + N that appears at the differential output. The evaluation board provides a series of jumpers that isolate this difference amplifier when it is not being used. To isolate the difference amp, set the jumpers as shown in Figure 13 and Figure 14.

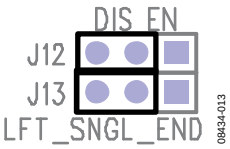

Figure 13. Left Single-Ended Disabled

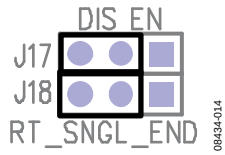

Figure 14. Right Single-Ended Disabled

To use the single-ended output, set the jumpers as shown in Figure 15 and Figure 16.

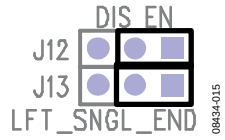

Figure 15. Left Single-Ended Enabled

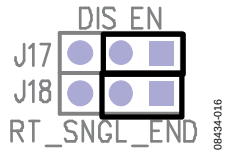

Figure 16. Right Single-Ended Enabled

CONFIGURING MONO MODE

To improve the SNR by 3 dB, the AD1955 can be configured in mono mode, combining the outputs from the two current output channels. To set up mono mode, follow these steps:

1. Cut LK4 and LK5 on the bottom of the board to disconnect the IOUTL+ and IOUTL− from the left I-to-V converter (see Figure 17).
2. Short LK8 and LK9 to sum IOUTL−/IOUTR+ and IOUTL+/IOUTR− (see Figure 17).

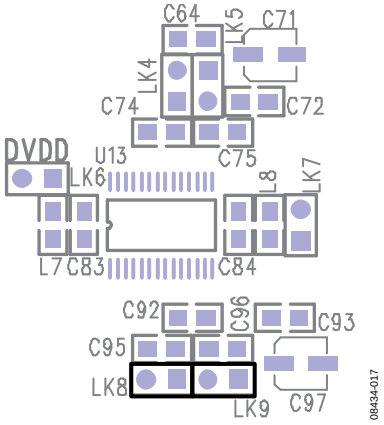

Figure 17. Links to Cut and Short for Mono Mode

3. Replace R80, R82, R95, and R97 with 1 kΩ, 0.1% resistors to adjust gain and bias (see Figure 18).

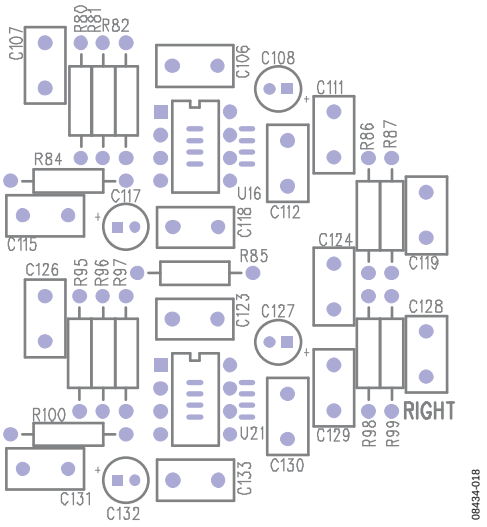

Figure 18. Location of R80, R82, R95, and R97

4. Set DAC Control Register 0, Bits[11:10] to 10 to select mono left input or to 11 to select mono right operation.
5. Mono audio appears at the right analog output of the evaluation board jacks.

SCHEMATICS AND ARTWORK

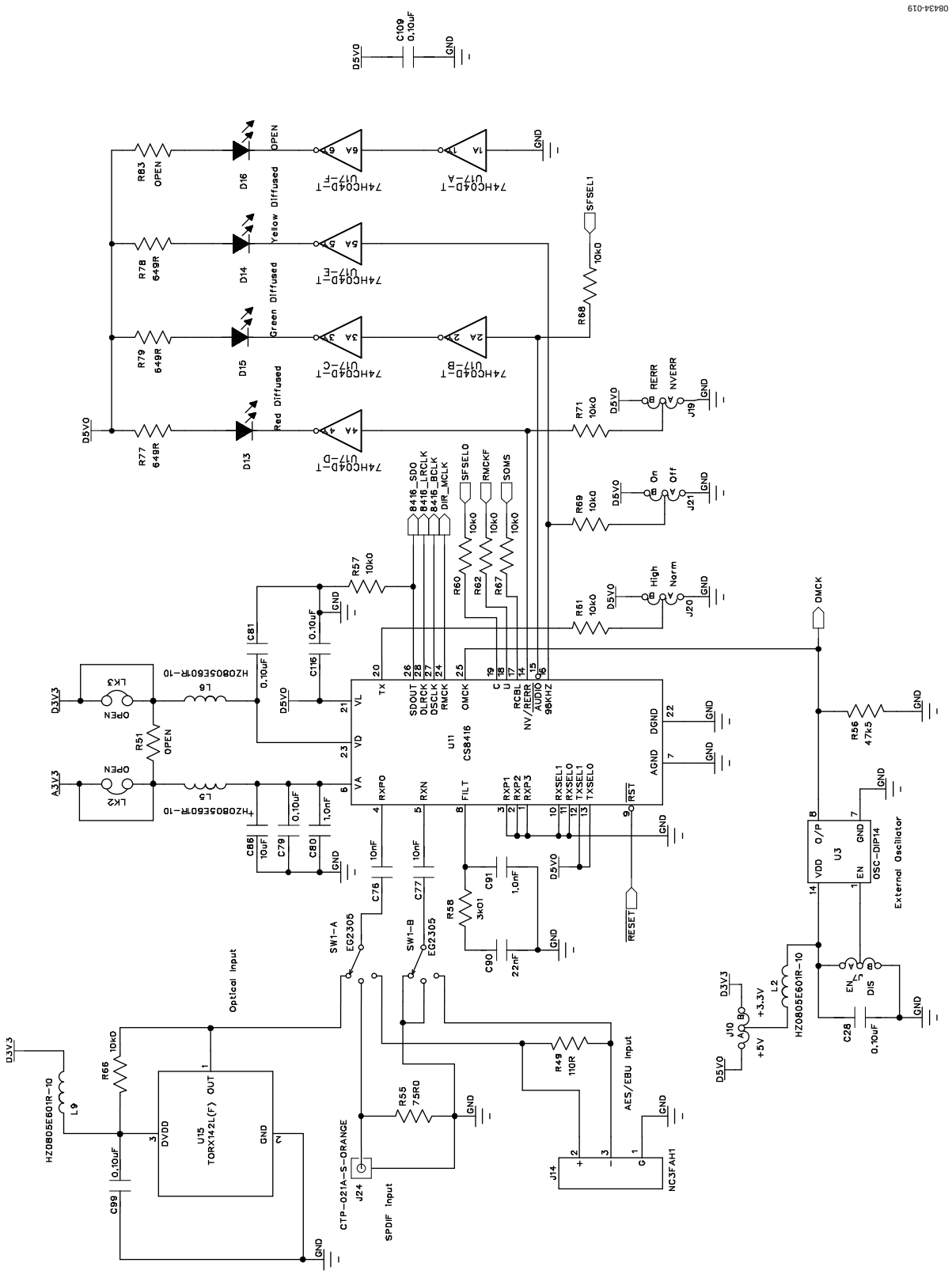

Figure 19. Schematic, Page 1—S/PDIF Receiver

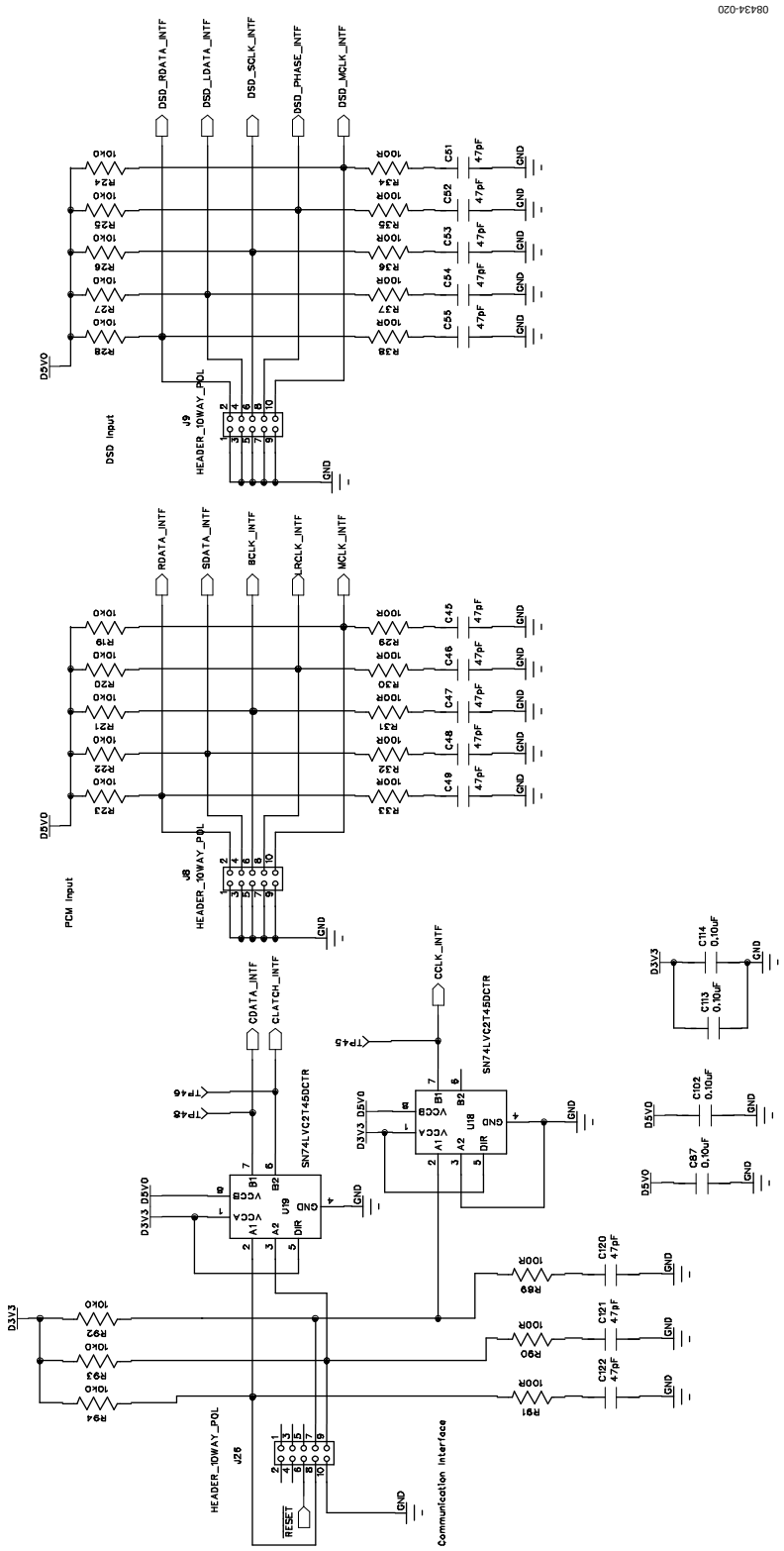

Figure 20. Schematic, Page 2—Serial Audio and USBi Headers

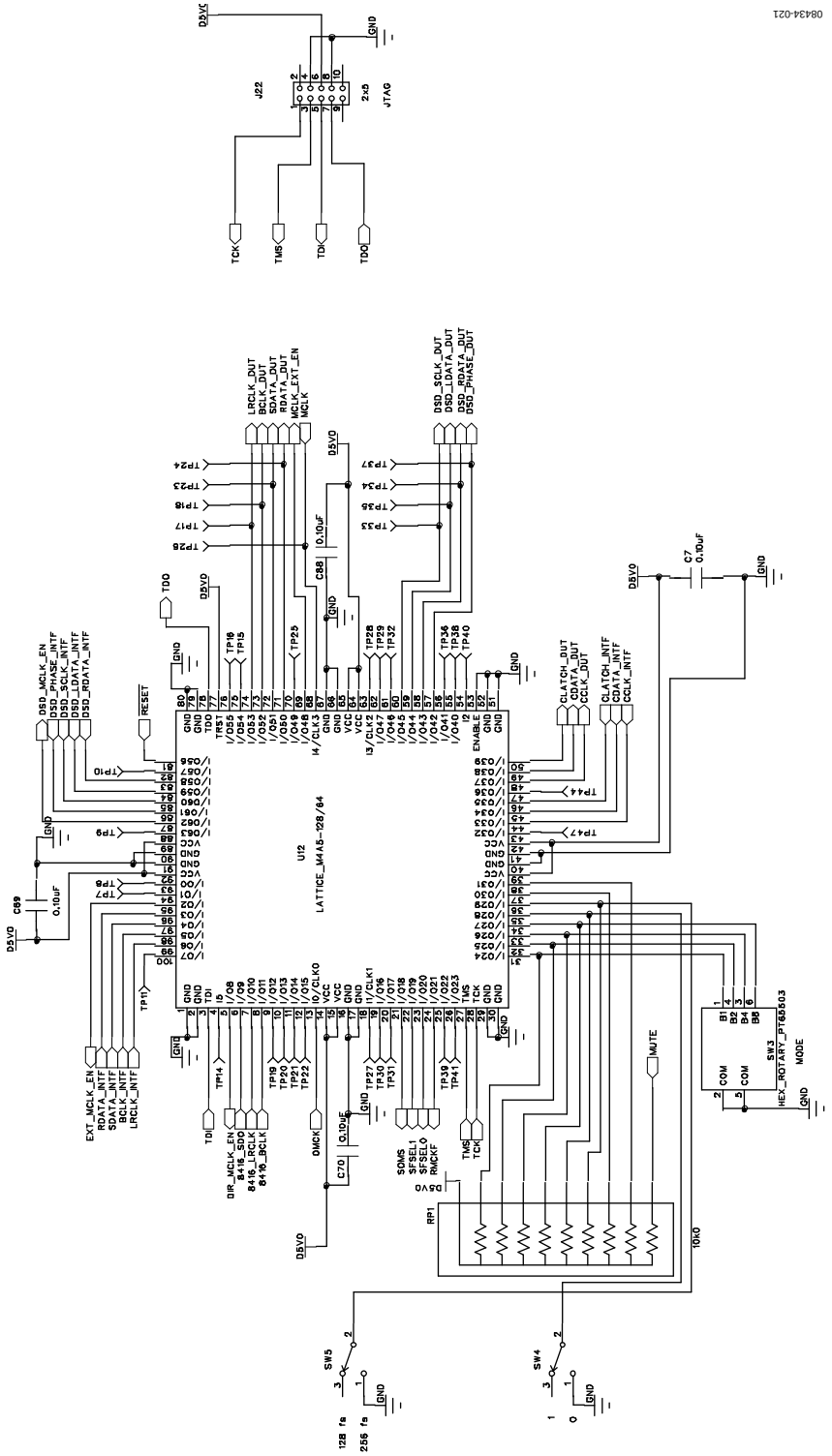

Figure 21. Schematic, Page 3—CPLD Routing Control

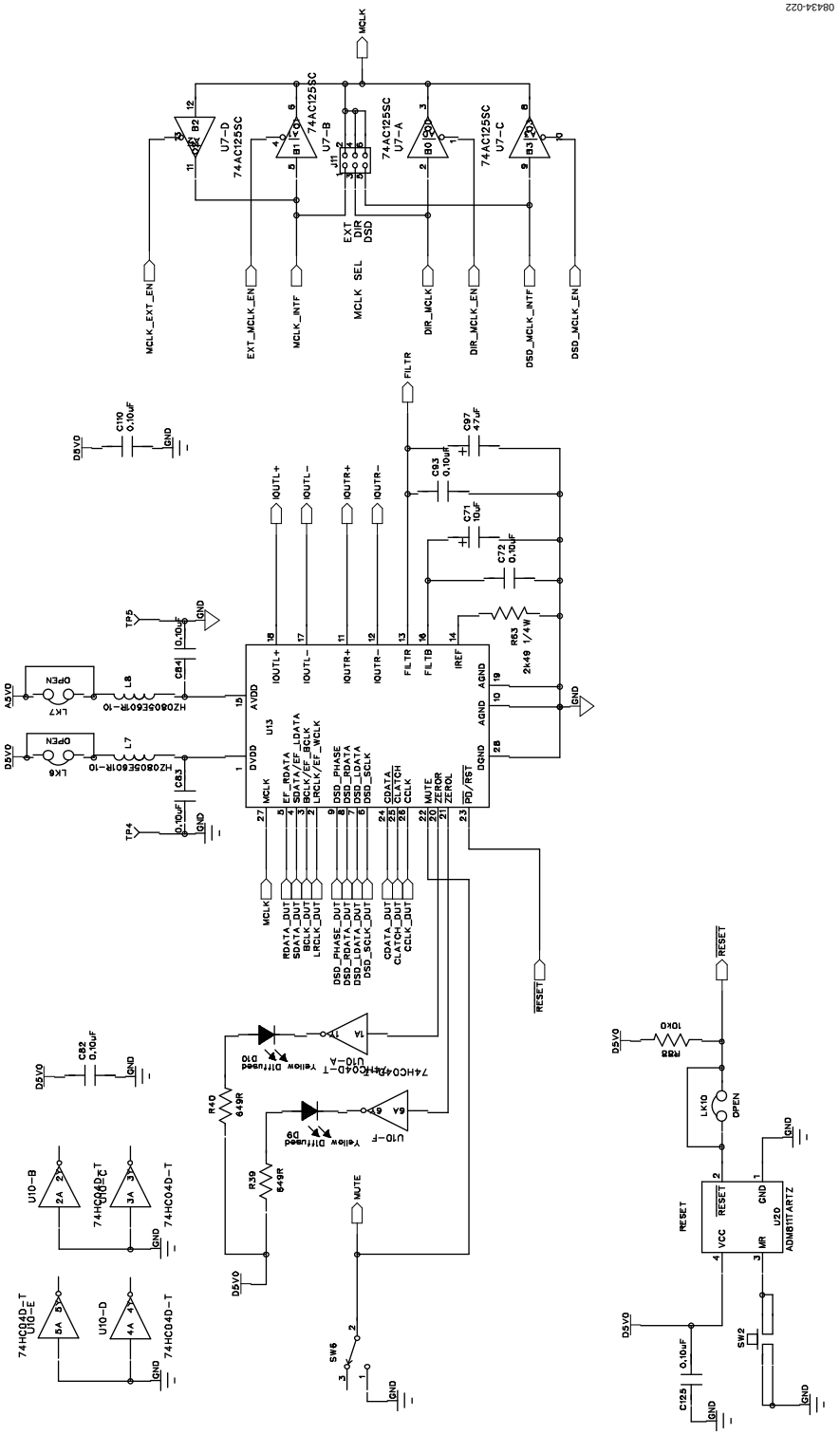

Figure 22. Schematic Page 4—AD1955 and MCLK Selector

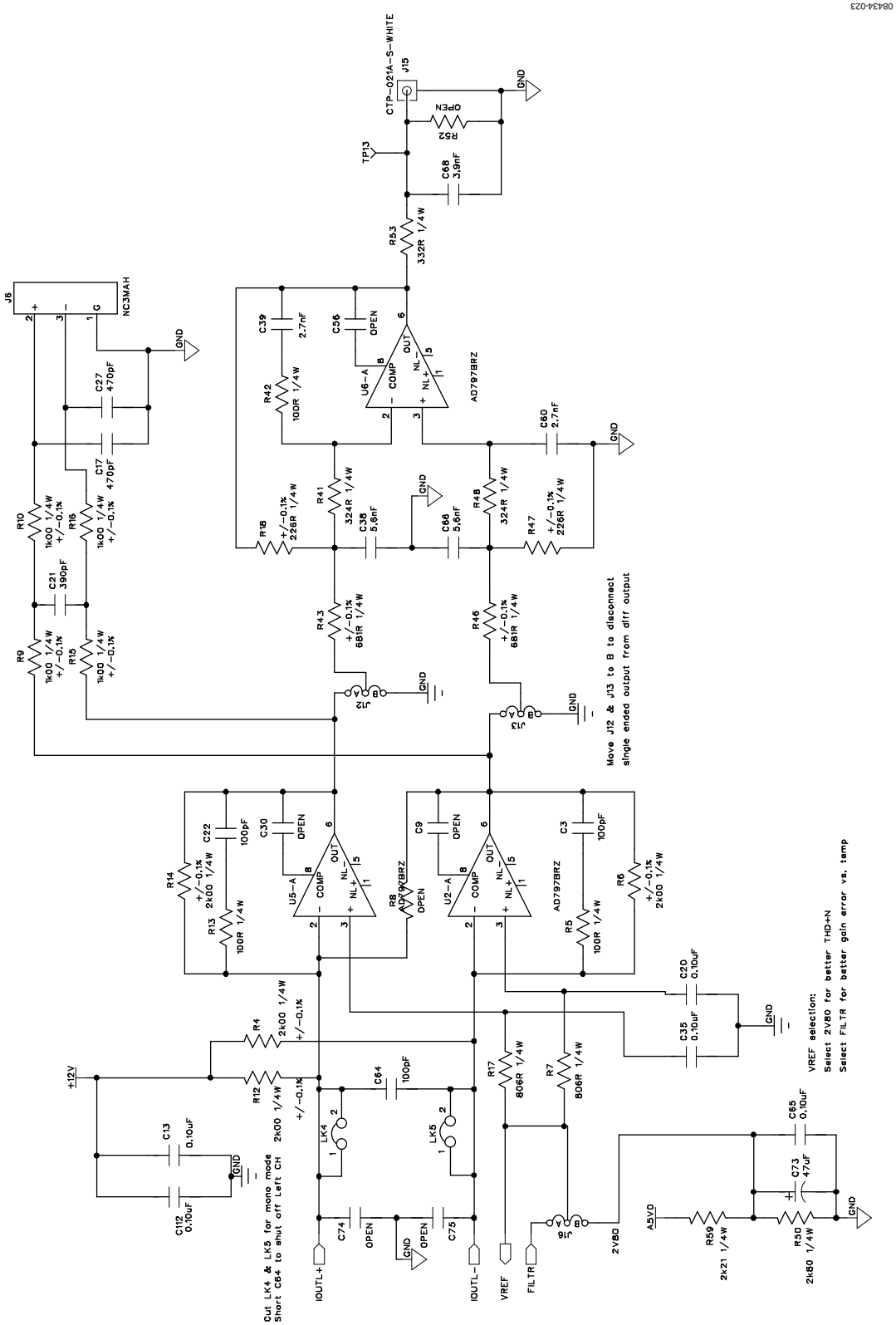

Figure 23. Schematic, Page 5—I/V Converter, Left Channel

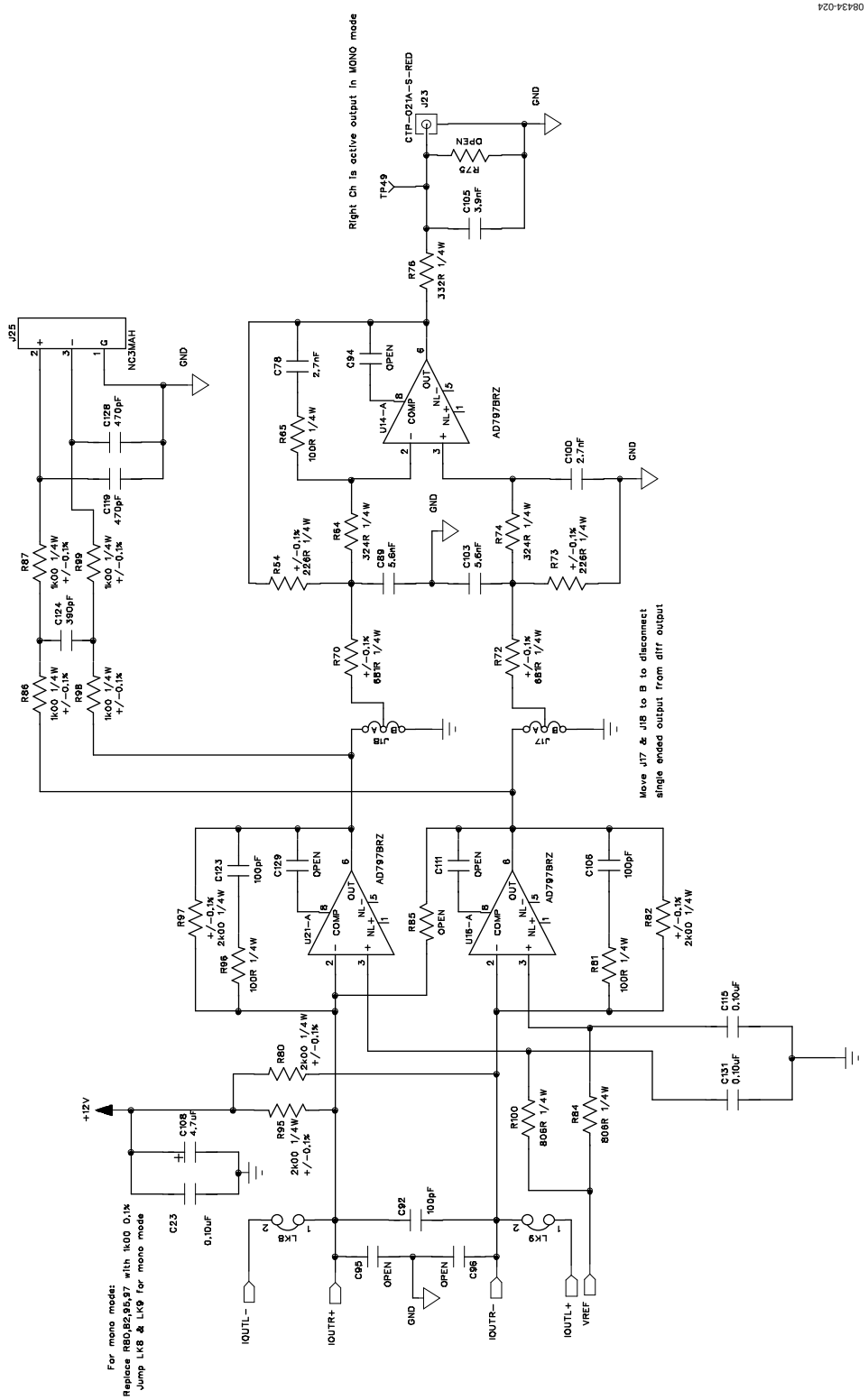

Figure 24. Schematic, Page 6—I/V Converter, Right Channel

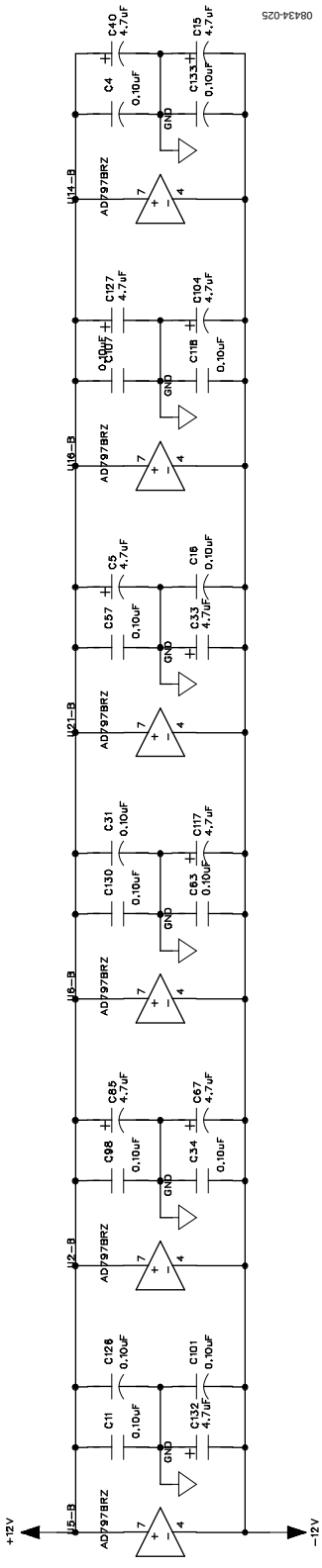

Figure 25. Schematic Page 7—Power Supply Decoupling

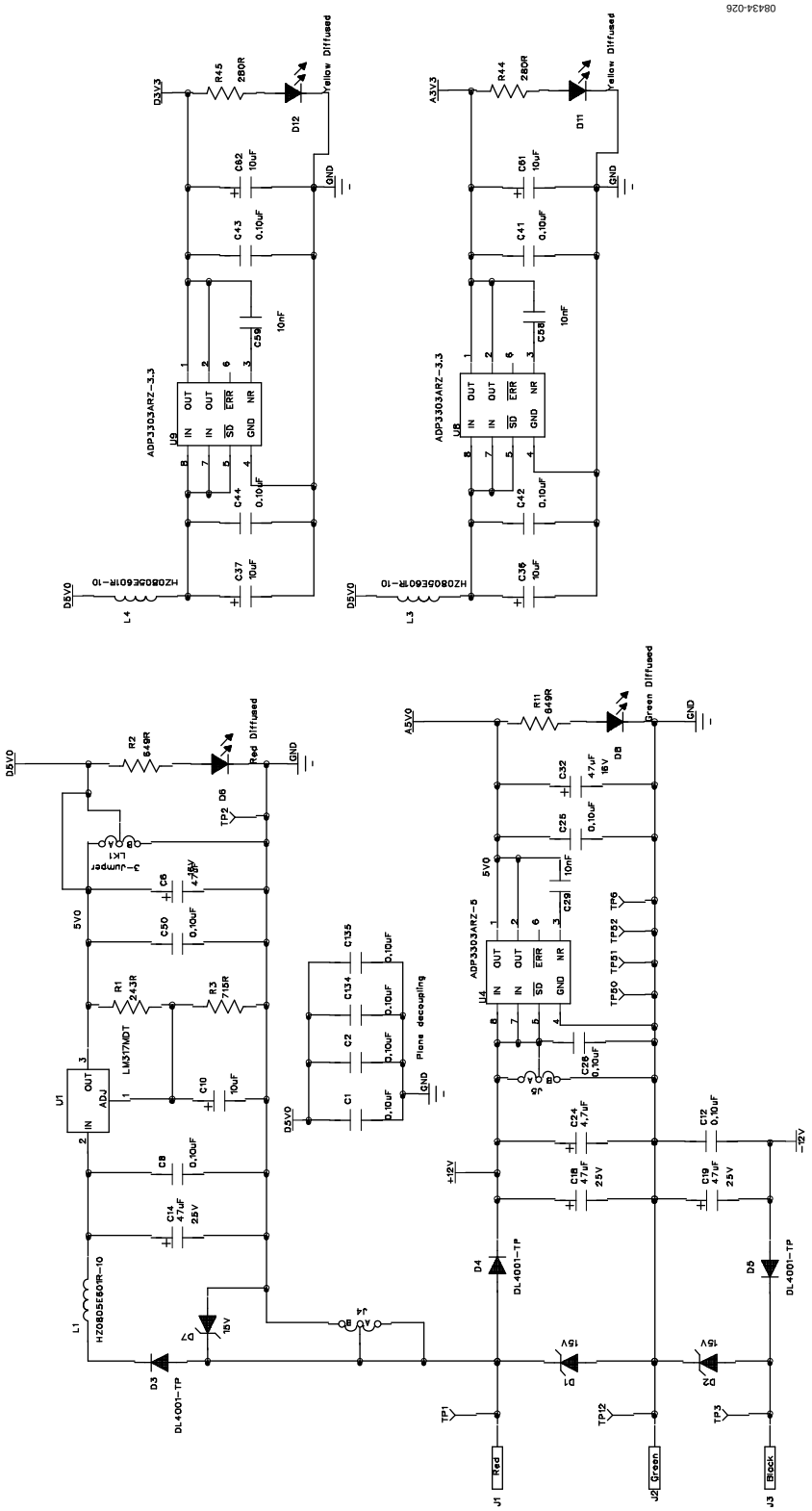

Figure 26. Schematic, Page 8—Power Supply Regulation

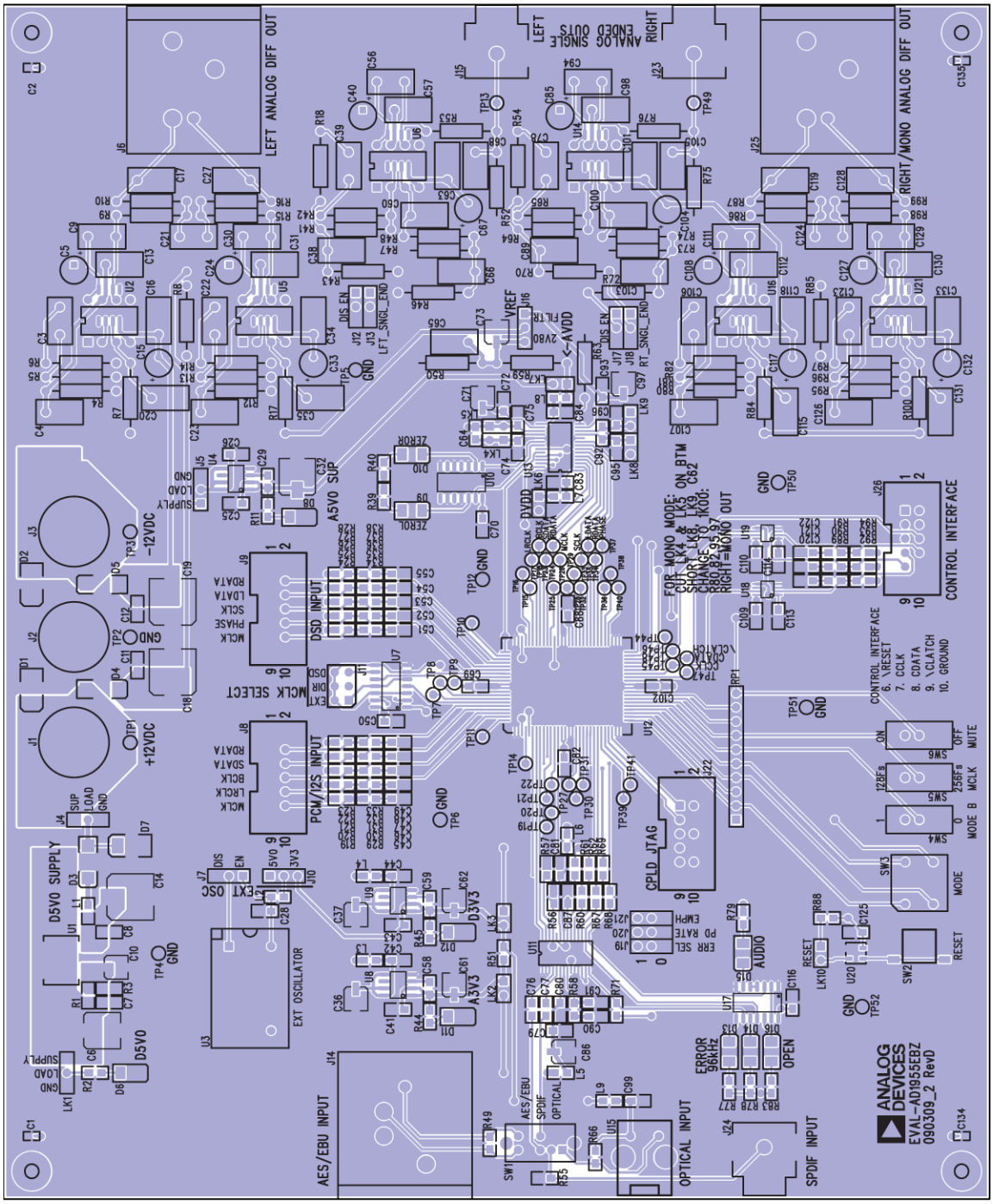

Figure 27. Top Assembly

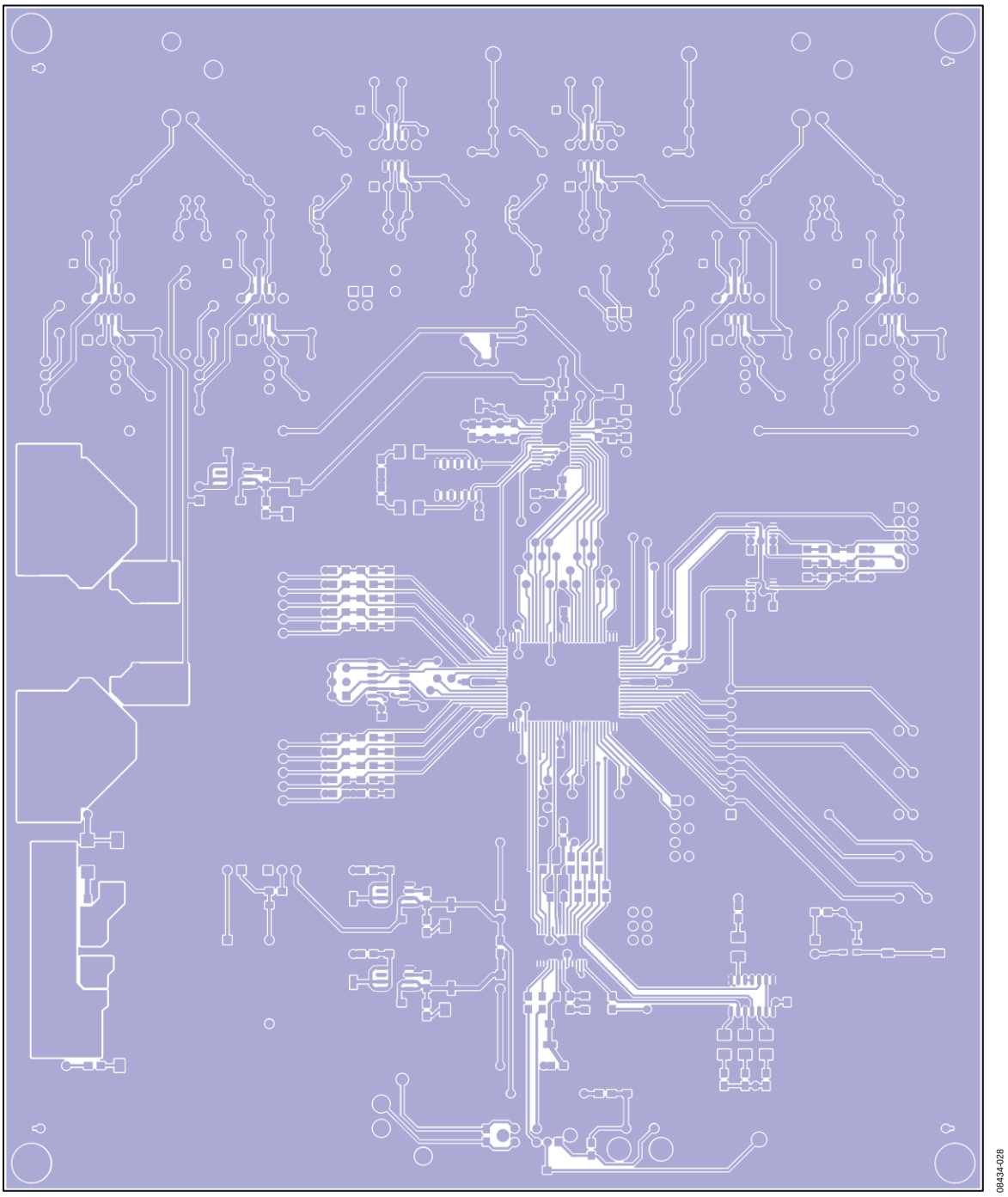

Figure 28. Top Layer Copper

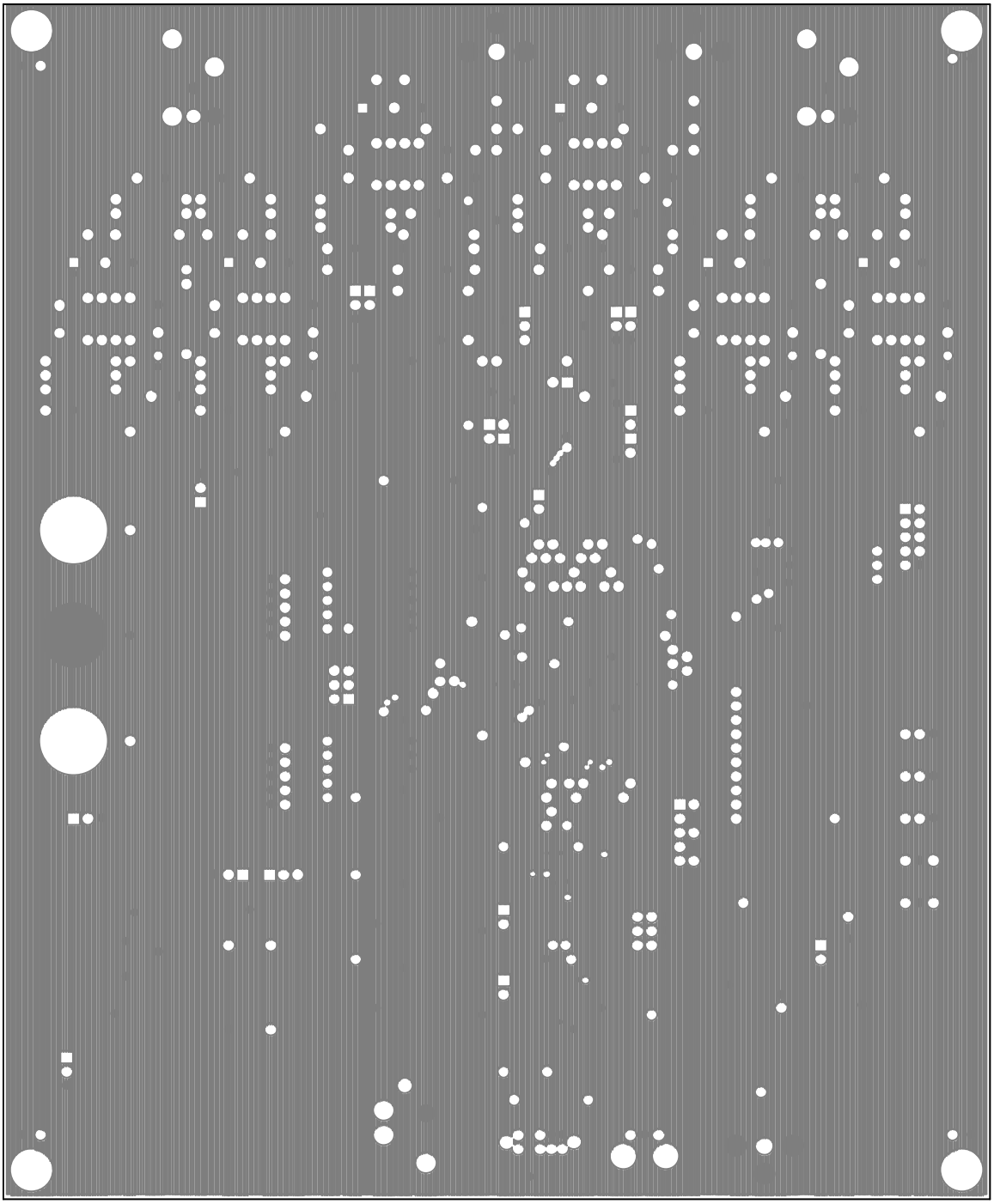

Figure 29. L2 Ground

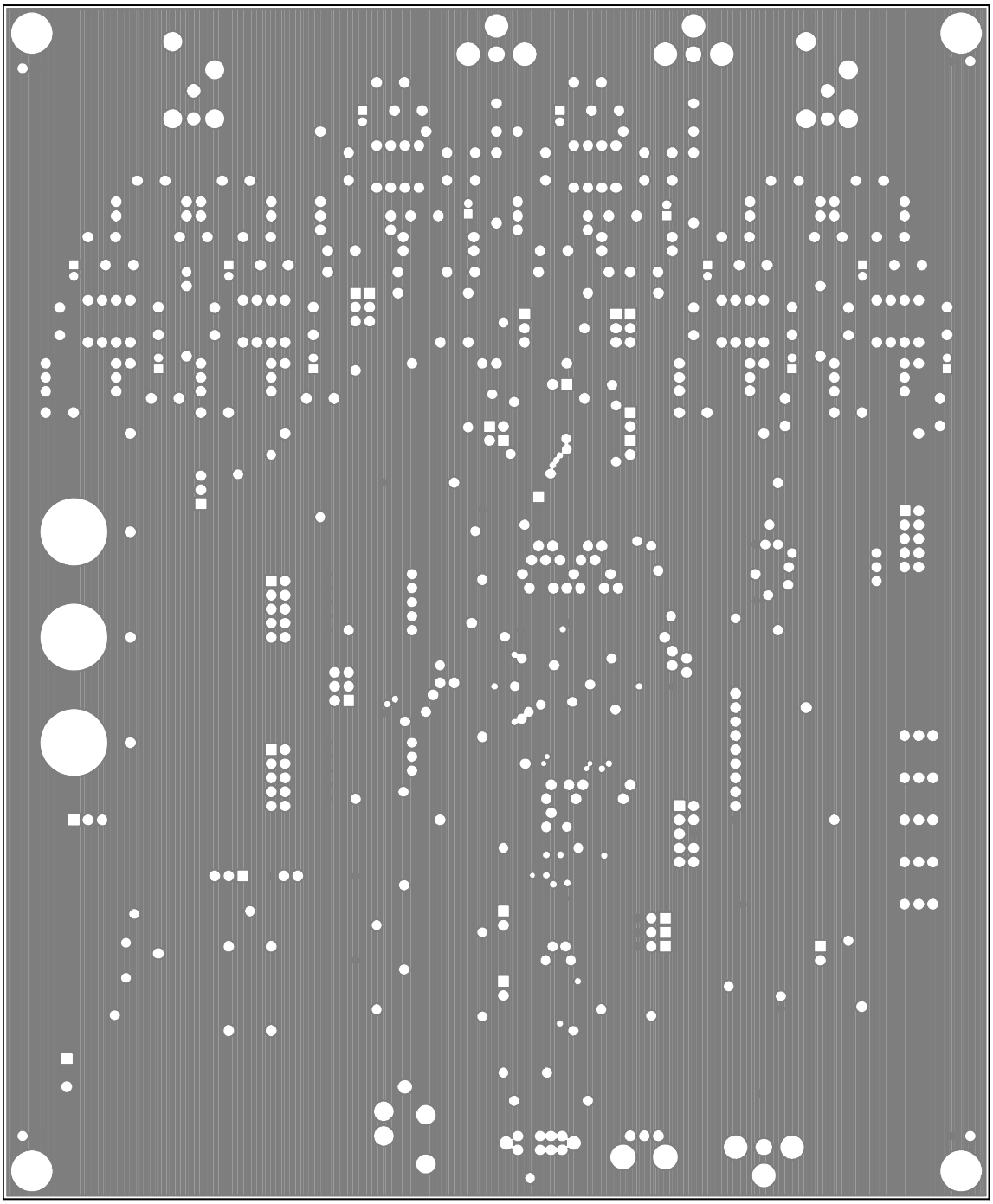

Figure 30. L3 Power

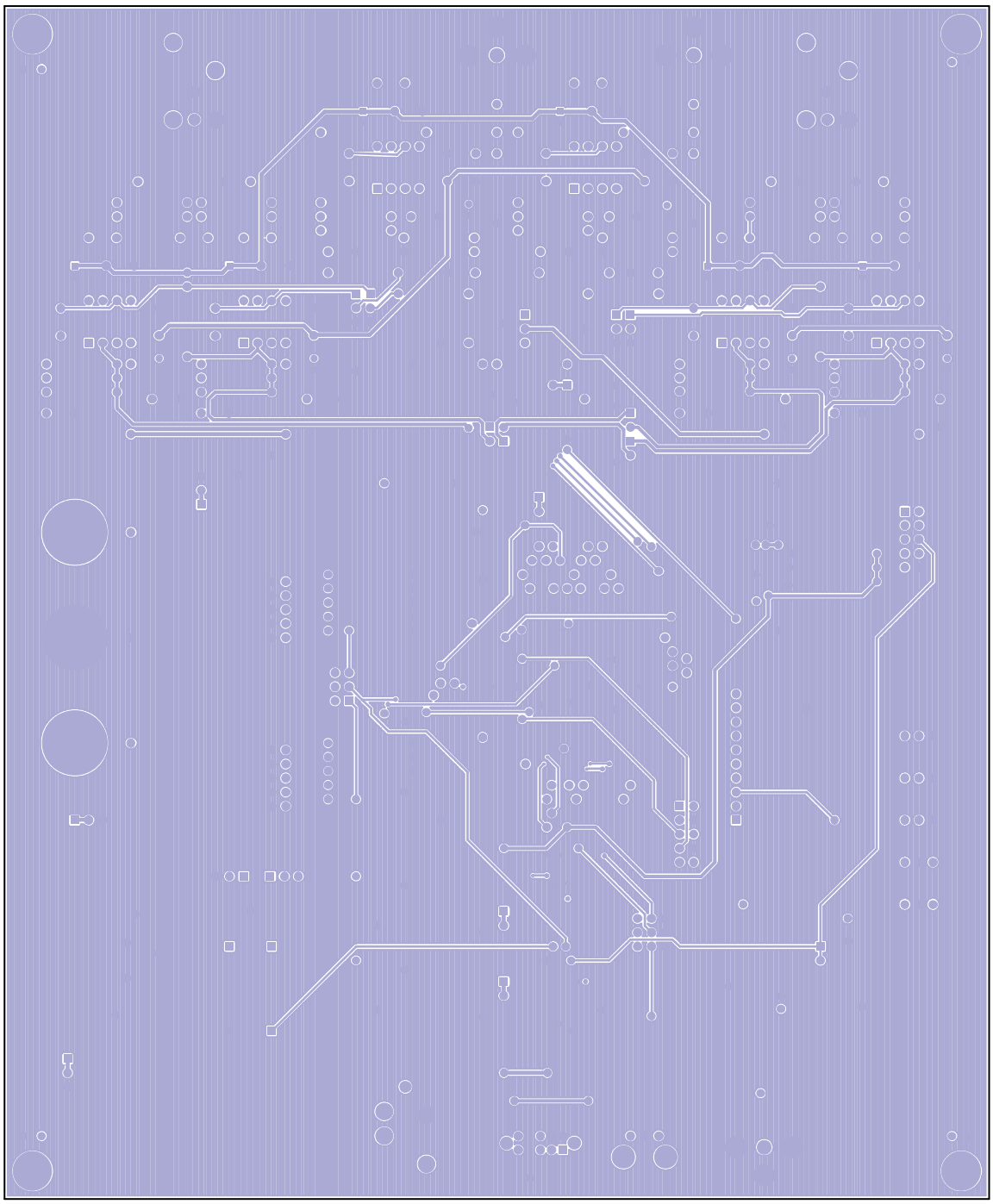

Figure 31. Bottom Copper

CPLD CODE

```
MODULE                    IF_Logic
TITLE   'AD1955 Eval. Board Interface Logic'

//-------------------------------------------------------------------------------
//

LIBRARY 'MACH';
   MACH_SLEW(FAST,1,MCLK);

DECLARATIONS

"INPUTS

   SW2_1, SW2_2, SW2_4, SW2_8
                          pin 31, 32, 33, 34;        // signal routing
   X8416_SDO, X8416_LRCLK, X8416_BCLK                                    pin 6, 7, 8;
                                                      // Data, clocks from 8416(1)
 //  X8416_SDO_AUX
                          pin 10;                 // Data from 8416(2)
   RDATA_INTF
                                                      pin 96;
                                                      // Data from Ext port
   DSD_RDATA_INTF, DSD_LDATA_INTF                                        pin 83, 84;
                                                      // Data from DSD port
   DSD_SCLK_INTF, DSD_PHASE_INTF                                         pin 85, 86;
   RESETB
                                                      pin 81;
                                                      // Reset (active low)
   CCLK_INTF, CDATA_INTF, CLATCH_INTF                                    pin 44, 45, 46;
                                                      // Data from SPI
   MCLK
                                                                         pin 68;
                                                                         // Master clock
// TDI, TMS, TCK
                          pin 3, 27, 28;                                 // JTAG input



"OUTPUTS

   X8416_M0, X8416_M1, X8416_M2, X8416_M3            pin 24, 23, 22, 21;        // 8416(1) and
8416(2) Mode Select
   CCLK_DUT, CDATA_DUT, CLATCH_DUT                                       pin 48, 49, 50;
                                                      // SPI data out to DUT
   DSD_PHASE_DUT, DSD_RDATA_DUT                                          pin 57, 58;
                                  // DSD data to DUT
   DSD_LDATA_DUT, DSD_SCLK_DUT
                          pin 59, 60;
   RDATA_DUT, SDATA_DUT, BCLK_DUT, LRCLK_DUT         pin 71, 72, 73, 74;        // Main data out
to DUT
```

```
// TDO
                                                                    pin 78;
                                                                    // JTAG output
   EXT_MCLK_EN
                                                    pin 95;
                                                    // enable external clock (active low)
   DIR_MCLK_EN
                                                    pin 5;
                                                    // enable direct clock (active low)
   MCLK_EXT_EN
                                                    pin 69;
   DSD_MCLK_EN
                                                    pin 87;


"INPUT/OUTPUTS
   SDATA_INTF, BCLK_INTF                                            pin 97, 98;
                                                    // Data from/to Ext port
   LRCLK_INTF
                                                    pin 99;
 //  X8416_LRCLK_AUX, X8416_BCLK_AUX                                  pin 11, 12;
// master or slave mode signals to 8416 aux


// unused pins

//   PIN_4
                                                    pin 4;
//   PIN_9
                                                    pin 9;
//   PIN_13
                                                    pin 13;
//   PIN_18, PIN_19, PIN_20
                          pin 18, 19, 20;
//   PIN_25, 26
                                                    pin 25, 26;
//   PIN_43
                                                    pin 43;
//   PIN_47
                                                    pin 47;
//   PIN_54, PIN_55, PIN_56
                          pin 54, 55, 56;
//   PIN_61, PIN_62, PIN_63
                          pin 61, 62, 63;


//   PIN_70
                                                    pin 70;
//   PIN_75, PIN_76
                          pin 75, 76;
//   PIN_82
                                                    pin 82;
//   PIN_88
                                                    pin 88;
//   PIN_93, PIN_94
                          pin 93, 94;
//   PIN_100
                                                    pin 100
```

```
//   PIN_35, PIN_36, PIN_38
                          pin 35, 36, 38

"NODES

   HCLK
                                                  node istype 'reg, buffer'; // MAKE THIS
CLOCK MASTER/128 = 192K
   ACLK, BCLK, CCLK, DCLK, ECLK, FCLK   node istype 'reg, buffer'; // clock divisions

// Registers for delaying the 8416 data in RJ and DSP modes
// such that it is output in the correct format
// to match the signal requirements for the AD1954.

    QA, QB, QC, QD, QE, QF                        node istype 'reg, buffer';
    QG, QH
                          node istype 'reg, buffer';
    Q24
                                                  node istype 'reg, buffer';
    QDSP
                          node istype 'reg, buffer';




"MACROS
// These are the eval board signal routing modes determined by the SW2 switch position

   D_14_1  = ( SW2_8 &  SW2_4 &  SW2_2 &  SW2_1);    // SW2 position 0         I2S
                            8416(1) input
   D_14_2  = ( SW2_8 &  SW2_4 &  SW2_2 & !SW2_1);    // SW2 position 1         LJ-24
   D_14_3  = ( SW2_8 &  SW2_4 & !SW2_2 &  SW2_1);    // SW2 position 2         DSP
   D_14_4  = ( SW2_8 &  SW2_4 & !SW2_2 & !SW2_1);    // SW2 position 3         RJ-24
   D_14_5  = ( SW2_8 & !SW2_4 &  SW2_2 &  SW2_1);    // SW2 position 4         RJ-16
   EXTDAT  = ( SW2_8 & !SW2_4 &  SW2_2 & !SW2_1);    // SW2 position 5         external port
select PCM and HDCD
   SACD    = ( SW2_8 & !SW2_4 & !SW2_2 &  SW2_1);    // SW2 position 6         HDCD
   D_14_192 = ( SW2_8 & !SW2_4 & !SW2_2 & !SW2_1);   // SW2 position 7         192K mode
 //  D_E_4   = (!SW2_8 &  SW2_4 &  SW2_2 &  SW2_1);  // SW2 position 8
 //  D_E_5   = (!SW2_8 &  SW2_4 &  SW2_2 & !SW2_1);  // SW2 position 9
 //  HDCD    = (!SW2_8 &  SW2_4 & !SW2_2 &  SW2_1);  // SW2 position A
 //  SACD    = (!SW2_8 &  SW2_4 & !SW2_2 & !SW2_1);  // SW2 position B
 //  D_14_192  = (!SW2_8 & !SW2_4 &  SW2_2 &  SW2_1);// SW2 position C
//   SPARE2_2  = (!SW2_8 & !SW2_4 &  SW2_2 & !SW2_1);// SW2 position D
//   SPARE2_1  = (!SW2_8 & !SW2_4 & !SW2_2 &  SW2_1);// SW2 position E
//   SPARE2_0  = (!SW2_8 & !SW2_4 & !SW2_2 & !SW2_1);// SW2 position F


EQUATIONS
```

```
//                                                                                clocks divided
from master clock
    ACLK.clk = MCLK;
    ACLK.d   = !ACLK;      //    master/2 frequency         use this as the bit clock in 192k
mode
    BCLK.clk = ACLK;
    BCLK.d = !BCLK;      //    master/4
    CCLK.clk = BCLK;
    CCLK.d = !CCLK;      //    master/8
    DCLK.clk = CCLK;
    DCLK.d = !DCLK;      //    master/16
    ECLK.clk = DCLK;
    ECLK.d = !ECLK;      //    master/32
    FCLK.clk = ECLK;
    FCLK.d = !FCLK;      //    master/64
    HCLK.clk = FCLK;
    HCLK.d = !HCLK;      //    master/128       should be a 192k clock, assuming input of 24.576
MHz



// Shift register for DSP, RJ_20, and RJ_24 modes from 8416
    [QH, QG, QF, QE, QD, QC, QB, QA] := [QG, QF, QE, QD, QC, QB, QA, X8416_SDO];
    Q24  := QH;                                                                    // Q24 returns
RJ-24 mode
    QDSP := QA;

    [QH, QG, QF, QE, QD, QC, QB, QA].clk = !X8416_BCLK;
    Q24.clk = X8416_BCLK;
    QDSP.clk = X8416_BCLK;



// Pass through SPI signals INVERTED
   CDATA_DUT  = !CDATA_INTF;
   CCLK_DUT   = !CCLK_INTF;
   CLATCH_DUT = !CLATCH_INTF;

// Master clock source enable
   DIR_MCLK_EN = !(D_14_1 # D_14_2 # D_14_3 # D_14_4 # D_14_5 # D_14_192);  //enable clock from
8416
   EXT_MCLK_EN = !EXTDAT;
   DSD_MCLK_EN = !SACD;
   MCLK_EXT_EN = !(D_14_1 # D_14_2 # D_14_3 # D_14_4 # D_14_5 # D_14_192);  //enable MCLK from
8416 to EXT

// normal data selection
   RDATA_DUT = (EXTDAT & RDATA_INTF);

   SDATA_DUT = X8416_SDO & (D_14_1 # D_14_2 # D_14_5)
                               # D_14_3 & QDSP
```

```
            # D_14_4 & Q24
                              # SDATA_INTF & EXTDAT;
//                            # D_14_192 & // 192K data output goes here

   BCLK_DUT  = !X8416_BCLK & (D_14_2 # D_14_4)
                              # X8416_BCLK & (D_14_1 # D_14_3 # D_14_5)
                              # BCLK_INTF & EXTDAT
            # D_14_192 & ACLK;                      //this should be okay for 192K mode

   LRCLK_DUT = X8416_LRCLK & (D_14_1 # D_14_2 # D_14_3 # D_14_4 # D_14_5)
                              # LRCLK_INTF & EXTDAT
            # D_14_192 & HCLK;  //this should be okay for 192K mode

// SACD data input
   DSD_PHASE_DUT = DSD_PHASE_INTF;
   DSD_RDATA_DUT = DSD_RDATA_INTF;
   DSD_LDATA_DUT = DSD_LDATA_INTF;
   DSD_SCLK_DUT  = DSD_SCLK_INTF;

// Configuration of the primary 8416, however these signals go to both 8416's
   X8416_M3 = !RESETB;
   X8416_M2 = !RESETB # D_14_3 # D_14_5;
   X8416_M1 = !RESETB # D_14_1 # D_14_192;
   X8416_M0 = !RESETB # D_14_5;  //both M1 and M2 must be high to set up the aux 8416 to slave
mode.

// Output of 8416 to EXT
   SDATA_INTF = SDATA_DUT;
   SDATA_INTF.oe = (D_14_1 # D_14_2 # D_14_3 # D_14_4 # D_14_5 # D_14_192);  //enable SDATA from
8416 to EXT

   BCLK_INTF  = BCLK_DUT;
   BCLK_INTF.oe  = (D_14_1 # D_14_2 # D_14_3 # D_14_4 # D_14_5 # D_14_192);  //enable BCLK from
8416 to EXT

   LRCLK_INTF = LRCLK_DUT;
   LRCLK_INTF.oe = (D_14_1 # D_14_2 # D_14_3 # D_14_4 # D_14_5 # D_14_192);  //enable LRCLK from
8416 to EXT

END IF_Logic
```

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Reference	Description	Manufacturer	Part Number
21	C4, C13, C16, C20, C23, C31, C34, C35, C57, C63, C65, C98, C101, C107, C112, C115, C118, C126, C130, C131, C133	Polyester film capacitor, 100°C, 5.0 mm, TH	BC Components	2222 370 22104
4	C1, C2, C134, C135	Multilayer ceramic capacitor, 16 V, X7R (0402)	Panasonic EC	ECJ-0EX1C104K
31	C7, C8, C1, C12, C25, C26, C28, C41 to C44, C50, C69, C70, C72, C79, C81 to C84, C87, C88, C93, C99, C102, C109, C110, C113, C114, C116, C125	Multilayer ceramic capacitor, 50 V, X7R (0805)	Panasonic EC	ECJ-2YB1H104K
2	C80, C91	Multilayer ceramic capacitor, 50 V, NP0 (0805)	Panasonic EC	ECJ-2VC1H102J
2	C64, C92	Multilayer ceramic capacitor, 50 V, NP0 (0805)	Panasonic EC	ECJ-2VC1H101J
4	C3, C22, C106, C123	Polypropylene film capacitor, 85°C, radial	Panasonic EC	ECQ-P1H101JZ
13	R29 to R38, R89 to R91	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF1000V
6	R5, R13, R42, R65, R81, R96	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-100R
23	R19 to R28, R57, R60 to R62, R66 to R69, R71, R88, R92 to R94	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF1002V
5	C29, C58, C59, C76, C77	Multilayer ceramic capacitor, 50 V, X7R (0805)	Panasonic EC	ECJ-2VB1H103K
7	C10, C36, C37, C61, C62, C71, C86	Aluminum electrolytic capacitor, FC, 105°C, SMD_B	Panasonic EC	EEE-FC1C100R
1	R49	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF1100V
8	R9, R10, R15, R16, R86, R87, R98, R99	0.25 W, 0.1%, metal film resistor	IRC	RC55LF-D-1K-B-B
3	D1, D2, D7	TVS Zener, 15 V, 600 W, SMB	ON Semiconductor	1SMB15AT3G
4	C39, C60, C78, C100	Polypropylene film capacitor, 85°C, radial	Panasonic EC	ECQ-P1H272GZ
4	R18, R47, R54, R73	0.25 W, 0.1%, metal film resistor	IRC	RC55LF-D-226R-B-B
1	C90	Multilayer ceramic capacitor, 50 V, X7R (0805)	Panasonic EC	ECJ-2VB1H223K
1	R1	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF2430V
2	R44, R45	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF2800V
8	R4, R6, R12, R14, R80, R82, R95, R97	0.25 W, 0.1%, metal film resistor	IRC	RC55LF-D-2K-B-B
1	R59	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-2K21
1	R63	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-2K49
1	R50	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-2K80
2	C68, C105	Polypropylene film, 85°C, radial	Panasonic EC	ECQ-P1H392GZ
4	R41, R48, R64, R74	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-324R
2	R53, R76	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-332R
2	C21, C124	Polypropylene film capacitor, 85°C, radial	Panasonic EC	ECQ-P1H391JZ
1	R58	Chip resistor, 1%,125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF3011V
12	C5, C15, C24, C33, C40, C67, C85, C104 C108, C117, C127, C132	Aluminum electrolytic capacitor, PW, 105°C, radial	Nichicon	UPW1V4R7MDD
4	C17, C27, C119, C128	Polypropylene film, 85°C, radial	Panasonic EC	ECQ-P1H471JZ
1	R56	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF4752V

Qty	Reference	Description	Manufacturer	Part Number
13	C45 to C49, C51 to C55, C120 to C122	Multilayer ceramic capacitor, 50 V, NP0 (0805)	Panasonic EC	ECJ-2VC1H470J
2	C73, C97	Aluminum electrolytic capacitor, FC, 105°C, radial	Panasonic EC	EEU-FC1C470
2	C6, C32	Aluminum electrolytic capacitor, FC, 105°C, SMD_D	Panasonic EC	EEE-FC1C470P
3	C14, C18, C19	Aluminum electrolytic capacitor, FC, 105°C, SMD_E	Panasonic EC	EEV-FC1E470P
4	C38, C66, C89, C103	Polypropylene film capacitor, 85°C, radial	Panasonic EC	ECQ-P1H562GZ
7	R2, R11, R39, R40, R77 to R79	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF6490V
4	R43, R46, R70, R72	0.25 W, 0.1%, metal film resistor	IRC	RC55LF-D-681R-B-B
1	R3	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF7150V
1	U7	IC buffer, quad, three-state, 14 SOIC	Fairchild Semiconductor	74AC125SC
2	U10, U17	IC inverter, hex, TTL/LSTTL, 14 SOIC	NXP Semi	74HC04D-T
1	R55	Chip resistor, 1%, 125 mW, thick film (0805)	Panasonic EC	ERJ-6ENF75R0V
4	R7, R17, R84, R100	0.25 W, 1%, metal film resistor	Yageo Corporation	MFR-25FBF-806R
1	U13	High performance, multibit, sigma-delta DAC with SACD playback	Analog Devices	AD1955ARSZ
6	U2, U5, U6, U14, U16, U21	Ultralow distortion, ultralow noise op amp	Analog Devices	AD797BRZ
1	U20	Microprocessor voltage supervisor	Analog Devices	ADM811TARTZ-REEL7
1	U4	Voltage regulator, low drop, low noise	Analog Devices	ADP3303ARZ-5
2	U8, U9	Voltage regulator, low drop, low noise	Analog Devices	ADP3303ARZ-3.3
1	J3	5-way binding post, black, uninsulated base, TH	Deltron	552-0100 BLK
1	J2	5-way binding post, mini, green, uninsulated base, TH	Deltron	552-0400 GRN
1	J1	5-way binding post, mini, red, uninsulated base, TH	Deltron	552-0500 RED
4	C74, C75, C95, C96	Do not populate	N/A	N/A
6	C9, C30, C56, C94, C111, C129	Do not populate	N/A	N/A
1	U11	192 kHz, AES3/S/PDIF receiver	Cirrus Logic	CS8416-DZZ
3	D3 to D5	Passivated rectifier, 1 A, 50 V, MELF	Micro Commercial	DL4001-TP
1	SW1	Switch slide, DP3T, PC MNT, L = 4 mm	E-Switch	EG2305
9	L1 to L9	Chip ferrite bead, 600 Ω at 100 MHz	Steward	HZ0805E601R-10
4	J8, J9, J22, J26	10-way shrouded, polarized header	3M	N2510-6002RB
1	J11	Connector header, 0.100 dual STR, 72 position	3M	PBC06DAAN; or cut PBC36DAAN
1	SW3	16-position rotary switch, hex	APEM	PT65503
10	J7, J10, J12, J13, J16 to J21	3-positioin SIP header	Sullins	PBC03SAAN; or cut PBC36SAAN
3	J4, J5, LK1	Do not populate	N/A	N/A
9	LK2 to LK10	Do not populate	N/A	N/A
1	U12	Complex programmable logic device, CPLD, high performance E2CMOS PLD	Lattice Semiconductor	M4A5-128/64-10YNC
2	D8, D15	Green, diffused, 10 millicandela, 565 nm (1206)	Lumex Opto	SML-LX1206GW-TR
1	D16	Do not populate	N/A	N/A

Qty	Reference	Description	Manufacturer	Part Number
2	D6, D13	Red, diffused, 6.0 millicandela, 635 nm (1206)	Lumex Opto	SML-LX1206IW-TR
5	D9 to D12, D14	Yellow, diffused, 4.0 millicandela, 585 nm (1206)	CML Innovative Tech	CMD15-21VYD/TR8
1	U1	3-terminal adjustable voltage regulator, DPak	STMicroelectronics	LM317MDT-TR
1	RP1	Resistor network, bussed 9-res	CTS Corp	770101103P
2	R51, R83	Do not populate	N/A	N/A
4	R8, R52, R75, R85	Do not populate	N/A	N/A
1	U3	Oscillator socket, full size, 4-pin	Aries Electronics	1107741
1	J24	RCA jack, PCB, TH mount, R/A, orange	Connect-Tech Products	CTP-021A-S-ORANGE
1	J23	RCA jack, PCB, TH mount, R/A, red	Connect-Tech Products	CTP-021A-S-RED
1	J15	RCA jack, PCB, TH mount, R/A, white	Connect-Tech Products	CTP-021A-S-WHITE
2	U18, U19	IC 2-bit dual bus, TXRX 8-SSOP	Texas Instruments	SN74LVC2T45DCTR
3	SW4 to SW6	SPDT slide switch, PC mount	E-Switch	EG1218
1	SW2	Tact switch, 6 mm, gull wing	Tyco/Alcoswitch	FSM6JSMA
1	U15	25 Mbps fiber optic receiving module with shutter	Toshiba	TORX142L(F)
50	TP1 to TP41, TP44 to TO52	Mini test point, white, 0.1" OD	Keystone Electronics	5002
1	J14	PC-mount, female XLR-3 receptacle	Neutrik	NC3FAH1
2	J6, J25	PC-mount, male XLR-3 receptacle	Neutrik	NC3MAH

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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