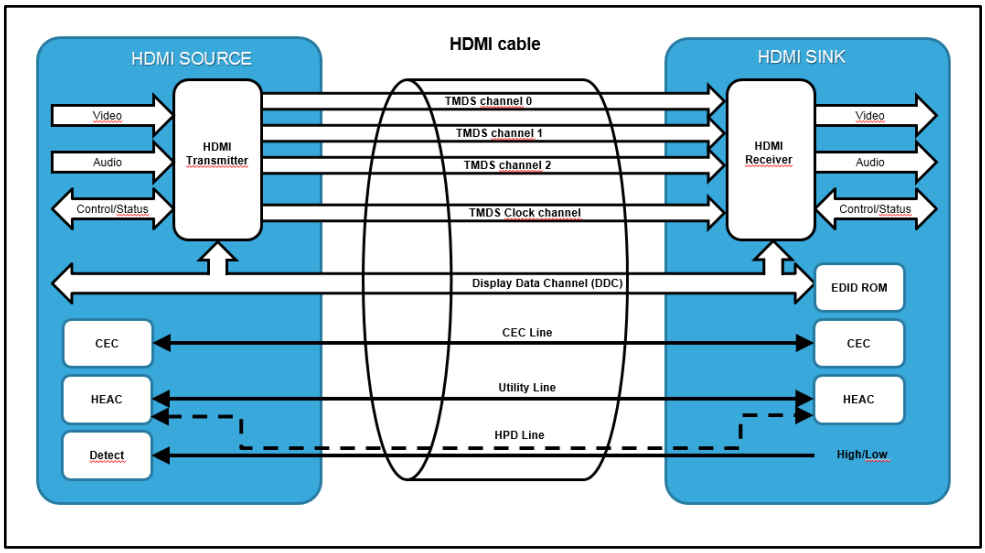
AN5121
Application note

HDMI ESD protection and signal conditioning products for STBs

Introduction

HDMI™ (High Definition Multimedia Interface) is a proprietary audio/video digital interface for transferring uncompressed video data and compressed or uncompressed audio data. This link is composed of one HDMI source and one HDMI sink linked together by an HDMI cable. As shown below, HDMI link is composed of 4 physically separate communication channels, which are TMDS, DDC, CEC (optional) and HEAC (optional).

Figure 1: HDMI block diagram



The TMDS channel is composed of 4 differential pairs, used to carry video, audio and auxiliary data with a maximum data throughput of 18 Gbps for HDMI 2.0, from the HDMI source to the HDMI sink.

The VESA DDC channel is composed of 2 lines based on I²C protocol. It is used for configuration and status exchange between a single source and a single sink. HDMI requires a maximum data rate of 100 kbps corresponding to I²C standard mode speed operation.

The optional CEC channel provides control functions between up to 10 HDMI devices. It is a one-wire bidirectional communication bus, based on CENELEC AV-link protocol.

The HEAC channel, composed of HEC and/or ARC channel, use the utility pin and the HPD pin to provide bidirectional 100 Mbps Ethernet link (HDMI Ethernet channel) and an audio channel (audio return channel) from the sink to the source.

This application note presents the HDMI™ port electrical characteristics for each channel and the constraints induced on ESD protection device choice.

Finally, ST offering in ESD protection for HDMI port and signal conditioning for DDC/CEC lines is presented.

Contents

1 EMI/EMC for STB: ESD test on system

All equipment that needs to comply with CISPR20:2006/EN55020:2006 or CISPR24:2010/EN55024:2010 standards must be able to withstand up to ±8 kV air discharge or ±4 kV contact discharge according to IEC61000-4-2 standard. The surge current waveform is given in the following figure and table.

Figure 2: IEC61000-4-2 typical current waveform, contact discharge

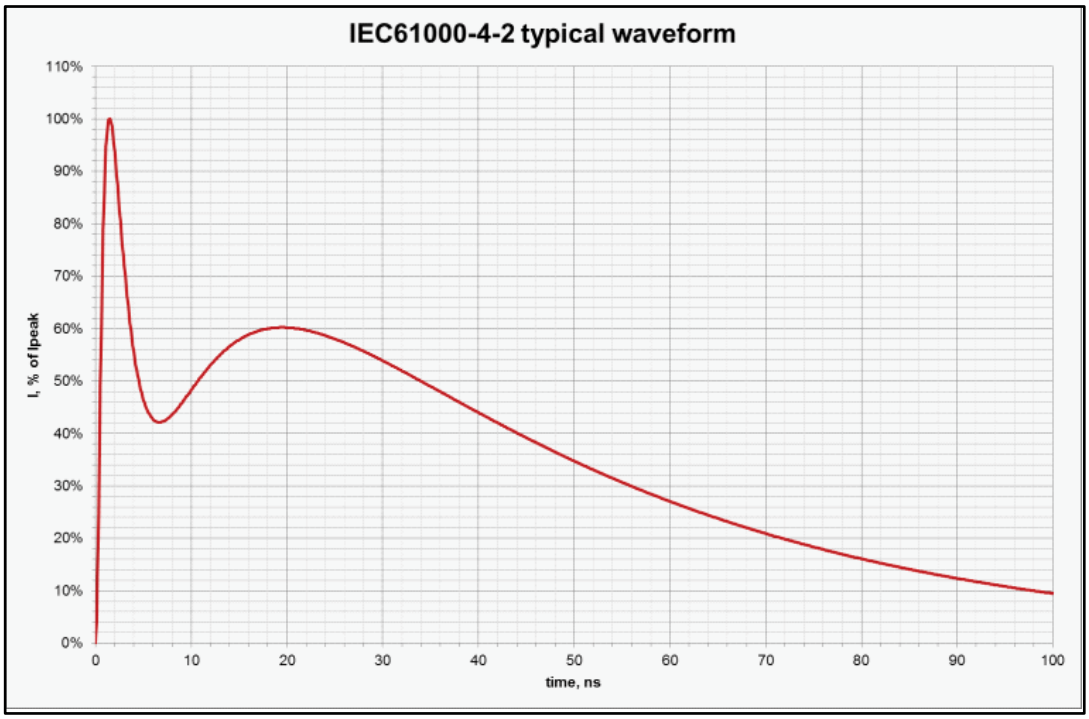


Table 1: IEC61000-4-2 ESD level, contact discharge

Level	Indicated voltage kV	First peak current of discharge ±15% A	Rise time t_r(±25%) ns	Current (±30%) at 30 ns A	Current (±30%) at 60 ns A
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

The reference point to measure the time for the current at 30 ns and 60 ns is the moment when the current first reached 10% of the discharge current first peak. The rise time, t_r is the time interval between 10% and 90% value of first peak current.

The equipment must keep on operating properly after the test. No loss of function is allowed after the test when the system is used properly, only failures, causing temporary delay in processing and recovering automatically, are acceptable. No change of actual operating state, such as change of channel or stored data and settings, is allowed as a result of the application of the test. During the test, degradation of performance is allowed.

2 TMDS lines

2.1 HDMI 1.4 and 2.0 requirements

2.1.1 Data rate

HDMI link is composed of 4 high speed TMDS lanes: 3 dedicated to data, 1 dedicated to clock synchronization. The clock lane speed is 1/10th of data lane speed for a data rate lower than 3.4 Gbps, and 1/40th of data lane speed for a data rate between 3.4 Gbps and 6 Gbps. The data rate on HDMI TMDS lanes depends on video resolution, frame rate and color depth. The pixel clock rate versus video resolution is given in EIA/CEA 861 standard (*Table 2: "HDMI Source and Sink TMDS lane characteristic impedance"* in EIA/CEA 861-D).

2.1.2 Differential impedance

To ensure a good signal propagation minimizing signal distortion, the entire transmission channel must be impedance matched. The impedance is checked through TDR measurements for HDMI sink and cable. It is also checked on source side since HDMI 2.0 specification. The TDR rise time must be set to 200 ps defined between 10% and 90%.

Table 2: HDMI Source and Sink TMDS lane characteristic impedance

Data rate	Source		Sink	
	Through connector	Termination impedance	Through connector	Termination impedance
RD ≤ 3.4 Gbps	NA	NA	100 Ω ±15 %(1)	100 Ω ±10%
3.4 Gbps < RD ≤ 6 Gbps	100 Ω ±10%	75 Ω min.150 Ω max.	100 Ω ±15% (1)	100 Ω ±10%

Notes:

(1)Single excursion of 100 Ω ±25% for a duration less than 250 µs is admitted.

2.1.3 Eye diagram

The signal quality transmission is evaluated through eye diagram measurement. HDMI standard defines the eye diagram mask function of TMDS data rate. Eye diagrams are measured at HDMI connector output (TP1) for data rate lower than 3.4 Gbps, and at the end of reference cable (TP2_EQ) for data rate between 3.4 Gbps and 6 Gbps.

Figure 3: HDMI source test point for eye diagram

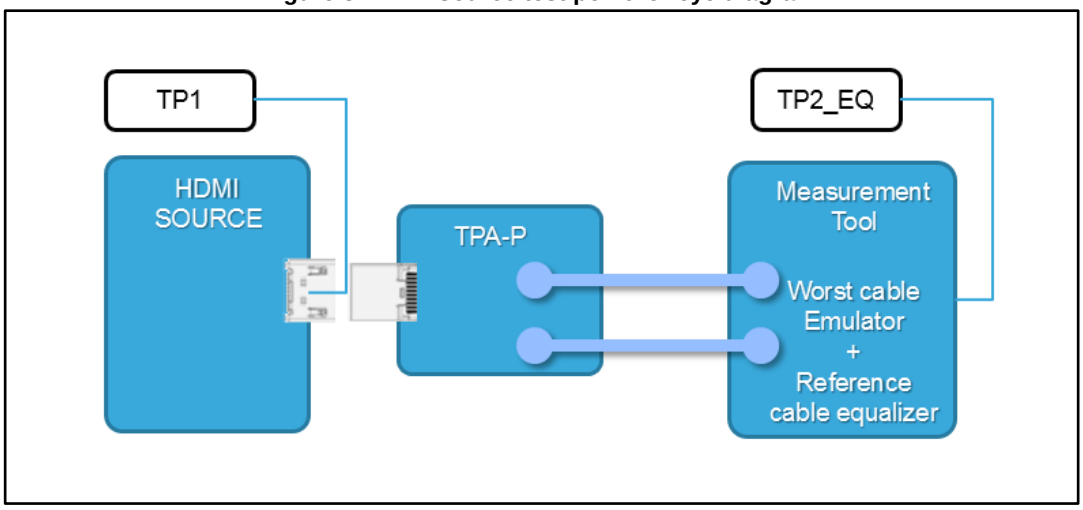
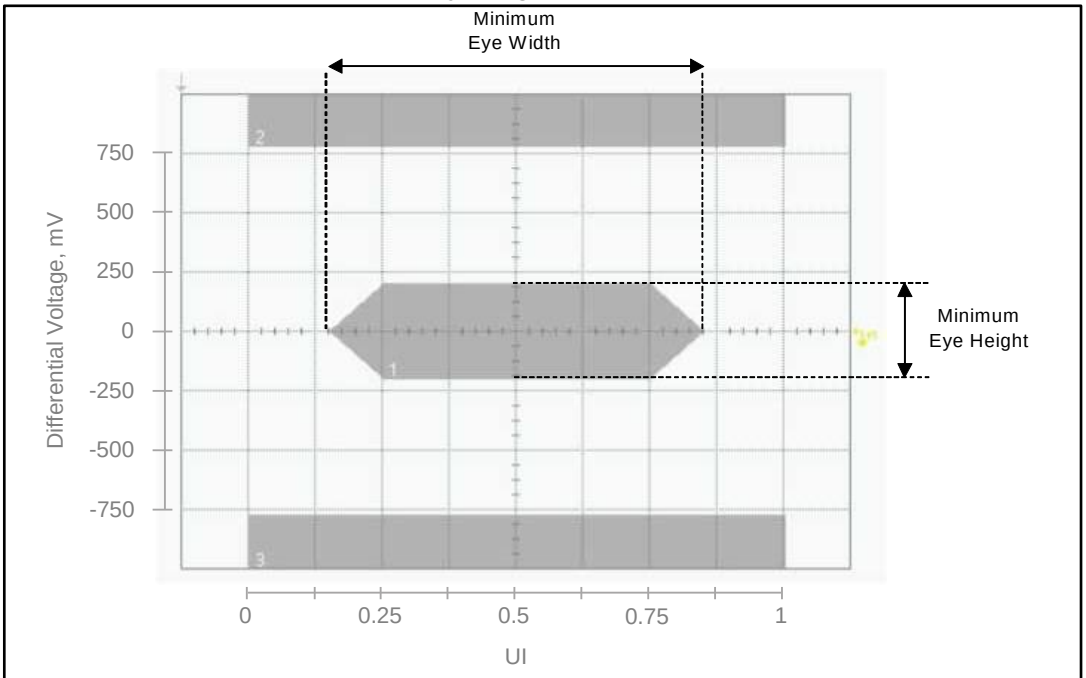
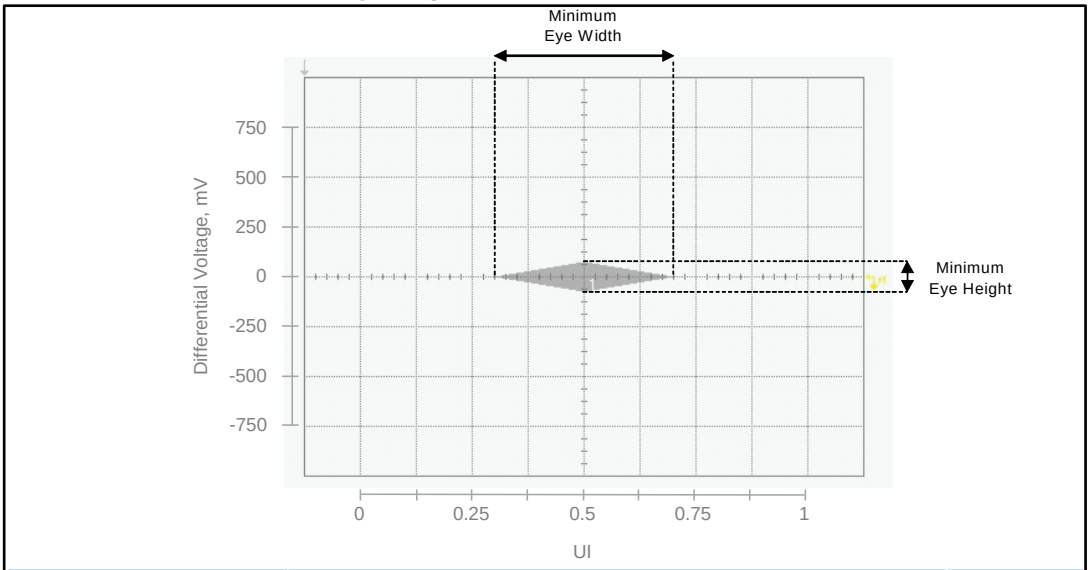


Figure 4: HDMI source eye diagram mask at TP1, Rbit ≤ 3.4 Gbps



Signal Characteristics	Minimal	Nominal	Maximum	Units
Eye Height	400		1560	mV
Eye Width	0.700			UI

Figure 5: HDMI source eye diagram mask at TP2_EQ, 3.4 Gbps < Rbit ≤ 6.0 Gbps



Signal characteristics	TMDS bit rate (Gbps)			Unit
	$3.4<R_{bit}<3.712$	$3.712<R_{bit}<5.94$	$5.94<R_{bit}<6.0$	
Eye Height	335	$-19.66R_{bit}^2+106.74R_{bit}+209.58$	150	mV
Eye Width	0.6	$-0.0332R_{bit}^2+0.2312R_{bit}+0.1998$	0.4	UI

2.2 PCB layout design

To ensure a good signal propagation minimizing signal distortion, the TMDS channel must be impedance matching. The PCB layout must be carefully designed with a differential impedance without ESD protection device as close as possible to 100 Ω unless specific requirements.

The ESD protection/EMI filter must be placed as close as possible to the connector for ESD safety reasons.

The tracks between ESD protection device and the line to be protected and between the protection device and the ground plane must be also as short as possible in order to minimize inductor effect on clamping voltage value. Indeed the track parasitic inductor adds an extra voltage to the clamping voltage of the ESD protection device.

Figure 6: Unoptimized ESD protection layout

Tracks between IO and ESD protection and between ESD protection and ground connection add extra voltage during ESD event

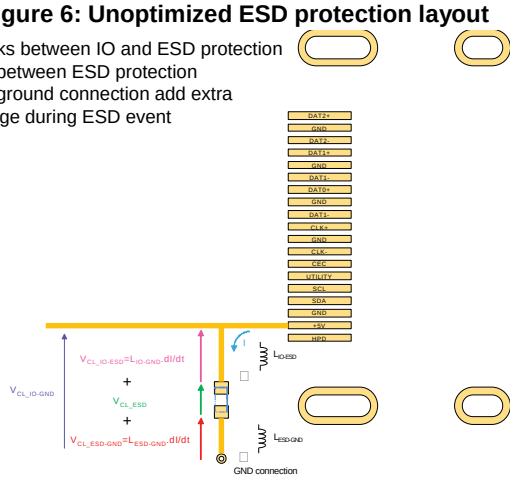
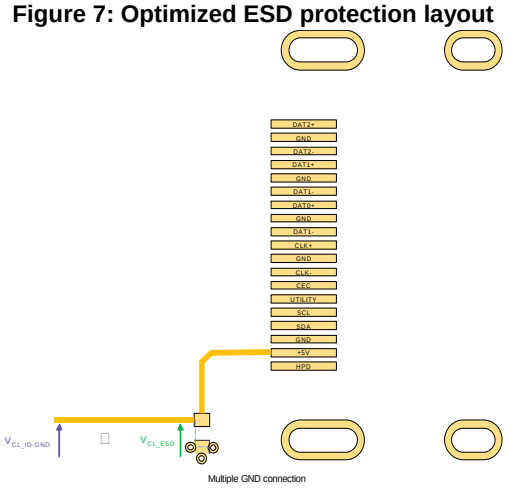


Figure 7: Optimized ESD protection layout



3 Control lines

3.1 DDC bus

3.1.1 HDMI standard requirements

The HDMI DDC bus is a point-to-point bidirectional communication link based on I²C bus specification. DDC bus meets I²C specifications in standard mode, meaning a maximum data rate of 100 kbit/s. I²C standard mode timing specifications are shown in *Table 3: "I²C timing requirements in standard mode (I²C specification, UM10204 rev.5)"*.

Table 3: I²C timing requirements in standard mode (I²C specification, UM10204 rev.5)

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
t_r	Rise time		1000	ns
t_f	Fall time		300	ns

All values are referenced to V_{IL}(max.)(0.3 x V_{DD}) and V_{IH}(min.)(0.7 x V_{DD}) levels.

HDMI devices must have DDC electrical characteristics complying with the values shown in *Table 4: "Maximum capacitance of DDC lines (HDMI 1.4, table 4-35)"*, *Table 5: "Maximum capacitance of DDC lines for automotive (HDMI 1.4, table 4-36)"* and *Table 6: "HDMI 1.4 pull-up resistors on DDC lines (HDMI 1.4, table 4-37)"*. That means a maximum total DDC bus capacitance of 1.5 nF in automotive applications (HDMI source + automotive cable + CE relay cable + automotive relay cable + HDMI sink), with SDA/SCL pull-up resistor between 1.5 kΩ and 2.0 kΩ on source side, and with SCL pull-up resistor of 47 kΩ ±10% on sink side.

Although HDMI standard specifies a maximum capacitance of 700 pF on DDC bus for cable, some on the market can have a higher capacitance value.

For instance, the capacitance SDA to ground or SCL to ground has been measured at 1.7 nF on a 15 meter cable.

Table 4: Maximum capacitance of DDC lines (HDMI 1.4, table 4-35)

Item	HDMI source	Cable assembly	HDMI sink
SDA-DDC/CEC ground	50 pF	700 pF	50 pF
SCL-DDC/CEC ground	50 pF	700 pF	50 pF

Table 5: Maximum capacitance of DDC lines for automotive (HDMI 1.4, table 4-36)

Item	HDMI source	Cable assembly			HDMI sink
		Automotive cable	CE relay cable	Automotive relay cable	
SDA-DDC/CEC ground	50 pF	700 pF	210 pF	490 pF	50 pF
SCL-DDC/CEC ground	50 pF	700 pF	210 pF	490 pF	50 pF

Table 6: HDMI 1.4 pull-up resistors on DDC lines (HDMI 1.4, table 4-37)

Item	Min.	Typ.	Max.
SDA and SCL source pull-up resistors	1.5 kΩ		2.0 kΩ
SCL sink pull-up resistor	42.3 kΩ	47 kΩ	51.7 kΩ

The failure to respect I²C timing and electrical requirements can generate interoperability issues at end customer side.

3.1.2 Benefits of switched pull-up on DDC bus

It is difficult to fulfill I²C timing specifications according to HDMI requirements in the worst conditions of DDC bus capacitance. The below equation gives the relation between rise time, pull-up resistor and bus capacitance for a rise time defined between 0.3 V_{DD} and 0.7 V_{DD}.

$$t_r = 0.85 * R_{PU} * C_{DDCBUS}$$

Considering a pull-up resistor of 2.0 kΩ with a bus capacitance of 800 pF, the rise time is 1.36 µs, higher than the 1 µs maximum value specified in HDMI standard.

Whereas a 1.5 kΩ pull-up resistor with the same 800 pF bus capacitance, the rise time is 1.02 µs, higher than the maximum allowed value.

HDMI standard allows the use of a switched pull-up circuit to manage high capacitance buses as described in I²C standard.

A switched pull-up circuit helps to fulfill HDMI and I²C timing requirements on DDC bus by temporarily decreasing the pull-up resistor value. Also it reduces the interoperability risk.

Figure 8: Rise time measurement with and without dynamic pull-up resistor, C_{LOAD} = 450 pF

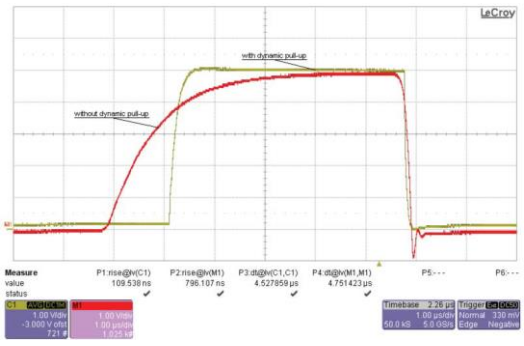
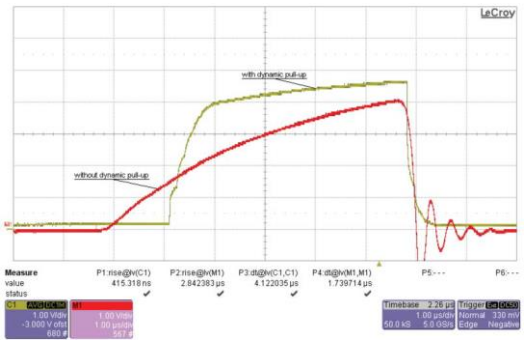


Figure 9: Rise time measurement with and without dynamic pull-up resistor, C_{LOAD} = 1.5 nF



3.2 +5 V power pin

The HDMI connector provides a pin allowing the source to supply +5 V to the cable and sink. All HDMI sources must be able to supply a minimum of 55 mA to the +5 V power pin, with an overcurrent protection of no more than 0.5 A. The voltage on the source output must be between 4.8 V and 5.3 V.

An HDMI sink must draw no more than 50 mA when powered off from +5 V power pin, and no more than 10 mA when powered on. The voltage on the sink input must be between 4.7 V and 5.3 V.

Figure 10: HDMI test points

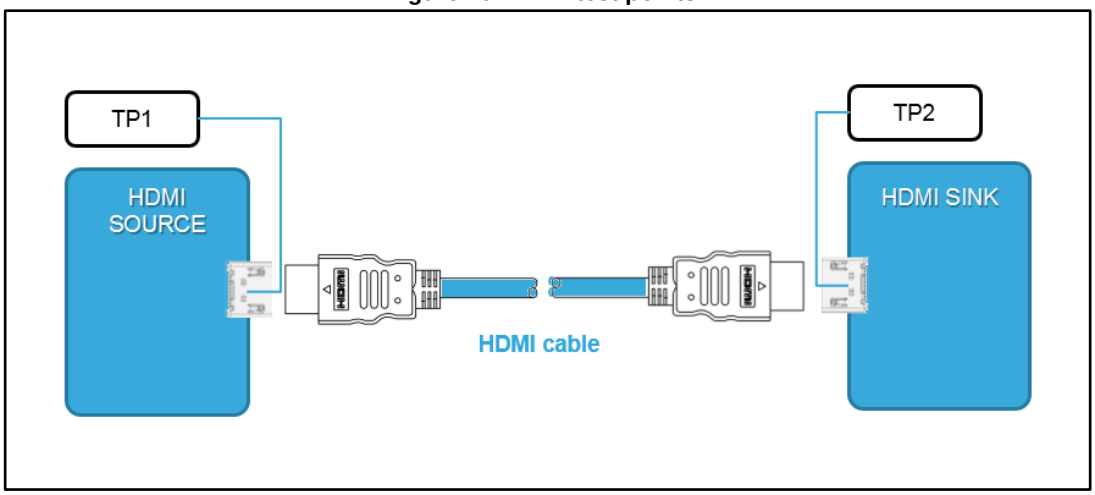


Table 7: +5 V power pin voltage

Item	Min.	Max.
Source output (TP1)	4.8 V	5.3 V
Sink input (TP2)	4.7 V	5.3 V

The +5 V power pin is used to supply power to the sink E-EDID EEPROM even if the sink is powered off or in standby mode.

3.3 HPD line

An HDMI source device uses an HPD line to detect if a sink device is connected to the end of HDMI cable. The HPD line is set to high level by the sink, sometimes through a 1 kΩ resistor connected to +5 V power pin.

On sink side, the HDP high level must be between 2.4 V and 5.3 V, on source side between 2.0 V and 5.3 V.

HEAC (HDMI Ethernet and audio return channel) optional feature can also use the HPD line.

4 ST offering for ESD protection of TMDS lanes:

4.1 HSP051-4M10

The HSP051-4M10 is a 4-line diode array ESD protection, suitable to protect TMDS lanes of HDMI connector. Its ultra-low IO/GND parasitic capacitance helps to minimize the impact of ESD protection device on TDR response as shown in *Figure 11: "HSP051-4M10 TDR measurements, tr 10%-90% = 200 ps (typical value)"*. The very high frequency bandwidth ensures a non-noticeable impact on eye diagram up to 3.4 Gbps (*Figure 12: "Eye diagram at 3.4 Gbps, without HSP051-4M10"*), and a small impact at 5.94 Gbps.

Figure 11: HSP051-4M10 TDR measurements, tr 10%-90% = 200 ps (typical value)

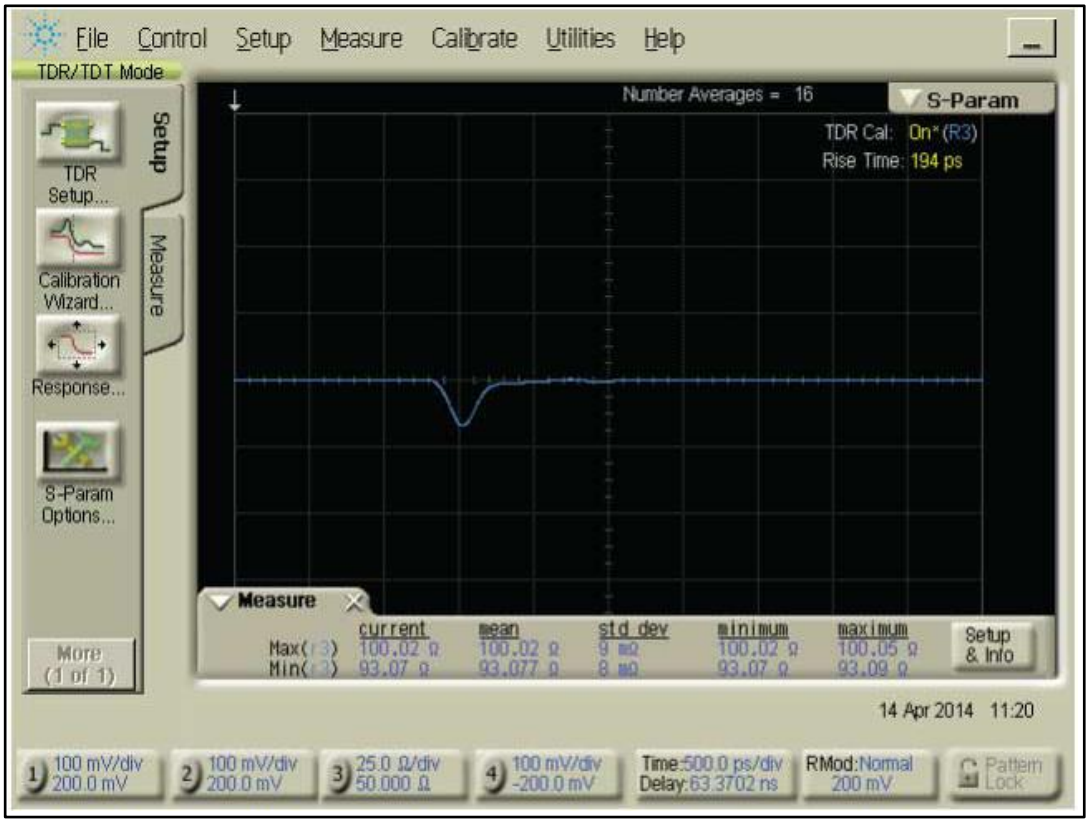


Figure 12: Eye diagram at 3.4 Gbps, without HSP051-4M10

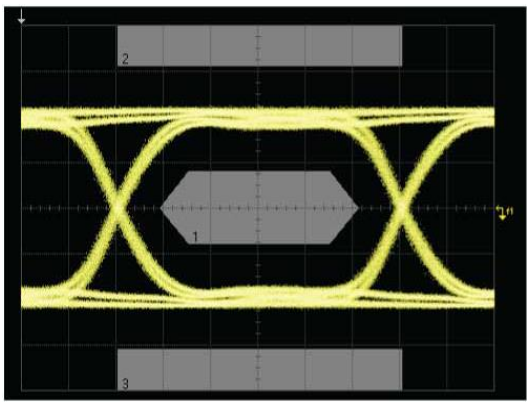


Figure 13: Eye diagram at 3.4 Gbps, with HSP051-4M10

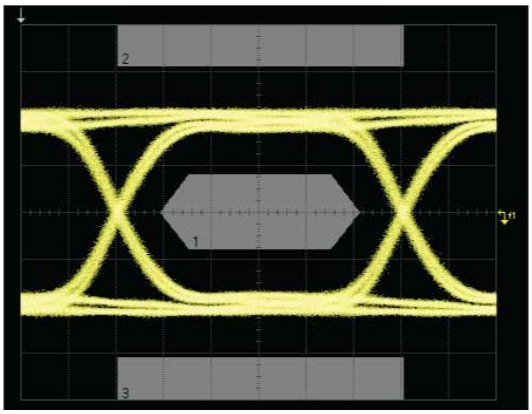


Figure 14: Eye diagram at 5.94 Gbps, without HSP051-4M10

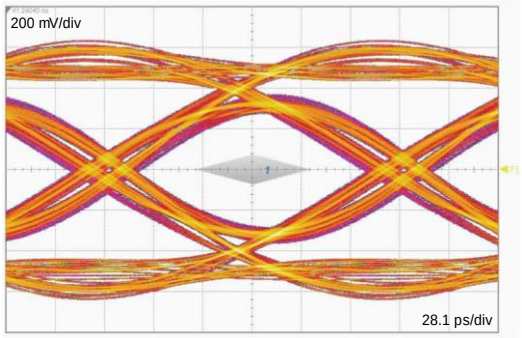
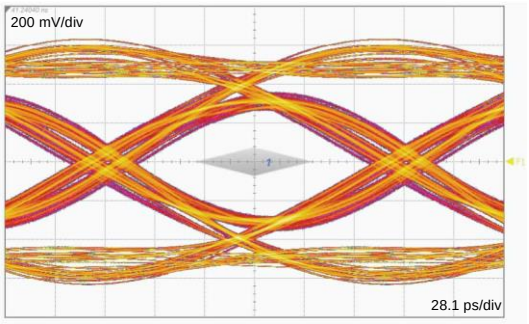


Figure 15: Eye diagram at 5.94 Gbps, with HSP051-4M10



HDMI TMDS lanes require two HSP051-4M10 for ESD protection. The typical electrical schematic is given in *Figure 16: "HSP051-4M10 electrical schematic"* and an example of layout in *Figure 17: "Layout example with 2 x HSP051-4M10"*.

Figure 16: HSP051-4M10 electrical schematic

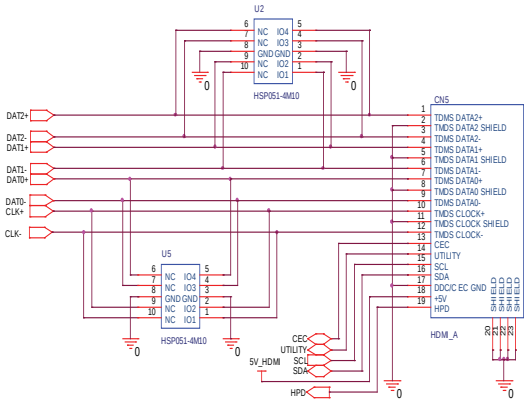
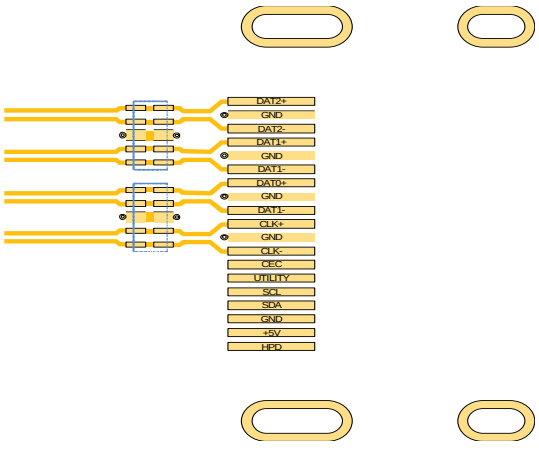


Figure 17: Layout example with 2 x HSP051-4M10



4.2 HSP053-4M5

The HSP053-4M5 is a 4-line diode array ESD protection, suitable to protect TMDS lanes of HDMI connector. Its ultra-low IO/GND parasitic capacitance helps to minimize the impact of ESD protection device on TDR response as shown in *Figure 18: "HSP053-4M5 TDR measurements, tr 10%-90% = 200 ps (typical value)"*. The very high frequency bandwidth ensures a non-noticeable impact on eye diagram up to 3.4 Gbps (*Figure 19: "Eye diagram at 3.4 Gbps, without HSP053-4M5"*), and a small impact at 5.94 Gbps.

Figure 18: HSP053-4M5 TDR measurements, tr 10%-90% = 200 ps (typical value)

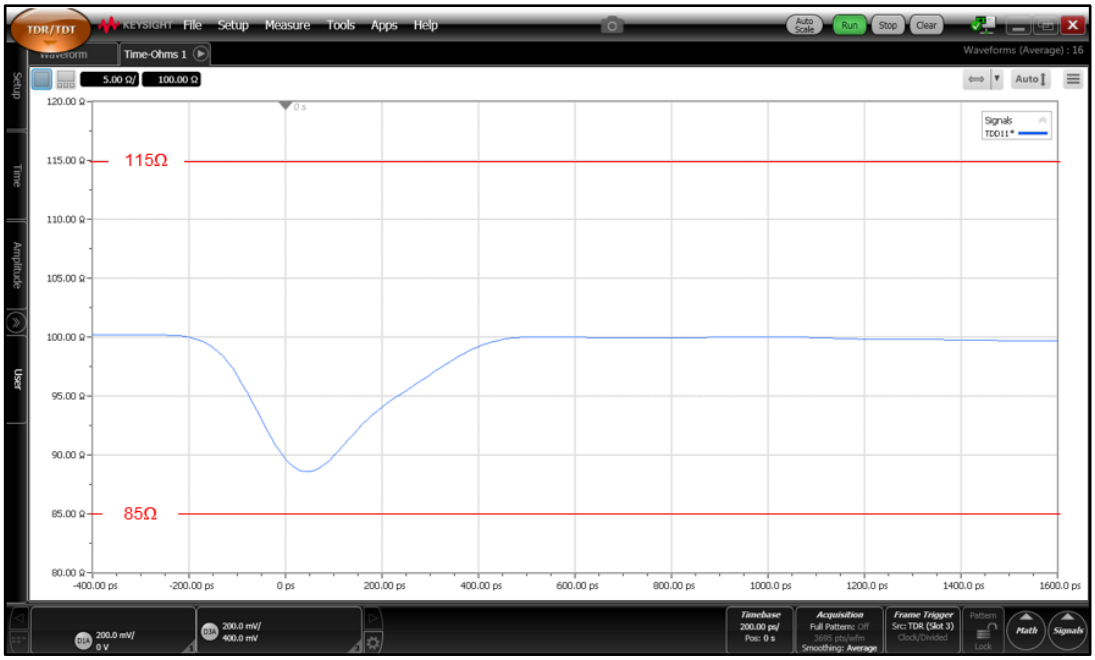


Figure 19: Eye diagram at 3.4 Gbps, without HSP053-4M5

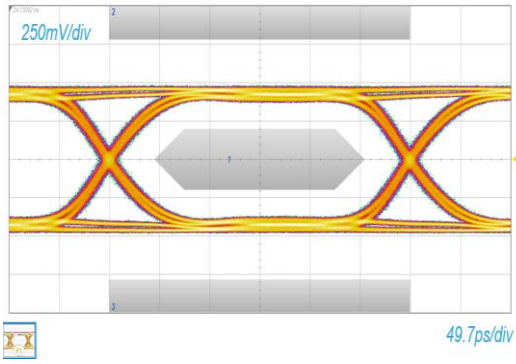


Figure 20: Eye diagram at 3.4 Gbps, with HSP053-4M5

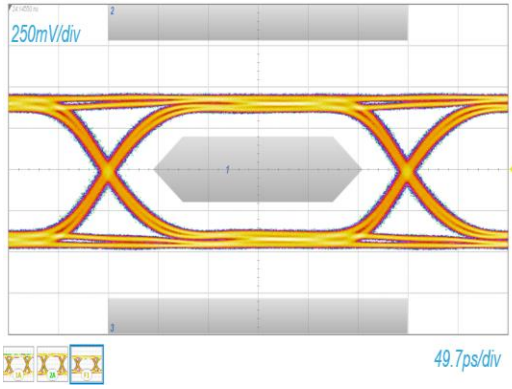


Figure 21: Eye diagram at 5.94 Gbps, without HSP053-4M5

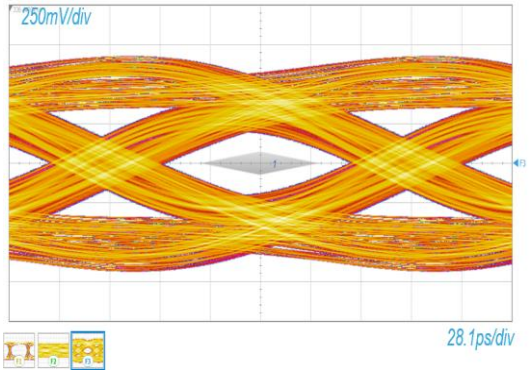
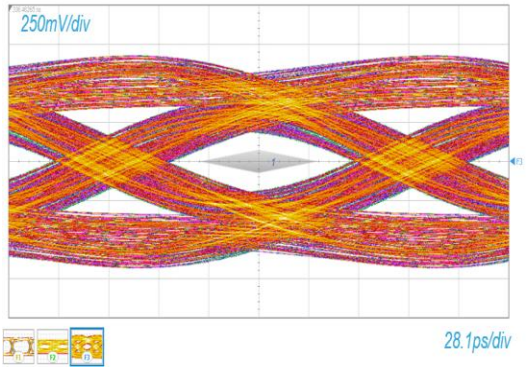


Figure 22: Eye diagram at 5.94 Gbps, with HSP053-4M5



HDMI TMDS lanes require two HSP053-4M5 for ESD protection. The typical electrical schematic is given in *Figure 23: "HSP053-4M5 electrical schematic"* and an example of layout in *Figure 24: "Layout example with 2 x HSP053-4M5"*.

Figure 23: HSP053-4M5 electrical schematic

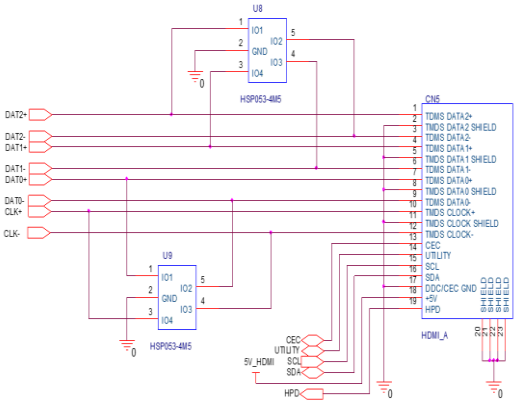
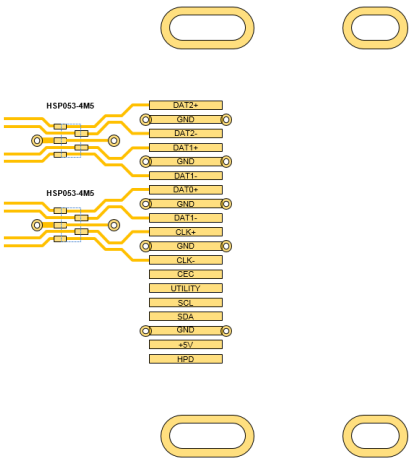


Figure 24: Layout example with 2 x HSP053-4M5



5 ST offer for control lines

5.1 HDMI2Cx family features

- ESD protection
  The HDMI2Cx product family able to withstand ± 8 kV contact discharge according to IEC61000-4-2 standard on connector pins and ± 2 kV HBM on other pins.
- DDC bus
  The HDMI2Cx product family integrates level shifter on DDC bus, allowing translating high level voltage from 5 V on cable side down to V_{DD_IC} on system side.
  It integrates dynamic pull-up resistors on DDC bus, allowing high capacitive cables to exceed HDMI standard specifications. Those dynamic pull-ups on cable side help to improve interoperability by ensuring a rise time on SDA and SCL lines compliant with HDMI and I²C specifications even with a capacitive load twice higher than HDMI requirements.
  The buffers on DDC bus ensure signal reshaping to improve signal quality transmission and ensure the compliance with capacitance measurements.
- HPD
  Unless specified, the HDMI2Cx product integrates a level shifter on HPD line, ensuring signal reshaping and voltage translation from 5 V on cable side to V_{DD_IC} on system side. The HPD line is pulled down through an integrated current source.
- +5 V power pin
  All HDMI2Cx products dedicated to source devices integrates on the +5 V power line a current limiter and a thermal protection to manage short circuit event on the +5 V HDMI connector pin.

5.2 HDMI2Cx for HDMI™ source devices

5.2.1 Control lines only

5.2.1.1 HDMI2C1-6C1

The HDMI2C1-6C1 is an integrated ESD protection and a signal-conditioning device for control lines of HDMI source. It provides current limitation and short-circuit protection on 5 V power pin. The HDMI2C1-6C1 is available in QFN18 leads, 500 µm pitch package.

Figure 25: HDMI2C1-6C1 package

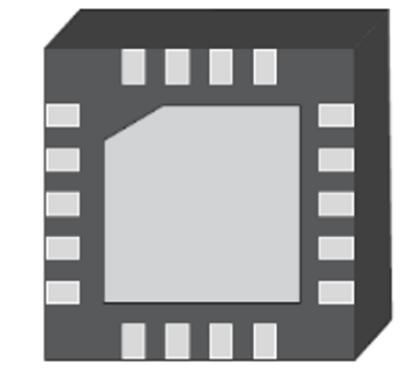
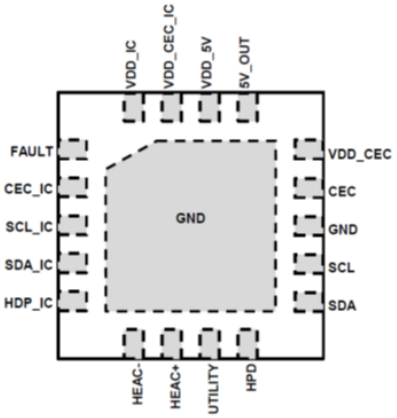


Figure 26: HDMI2C1-6C1 pinout, top view



The active low fault pin is used to indicate a short-circuit or an overtemperature protection activation on 5V_OUT pin.

The HDMI2C1-6C1 (*Figure 26: "HDMI2C1-6C1 pinout, top view"*) pinout provides an easy routing. The typical electrical schematic is given in *Figure 27: "HDMI2C1-6C1 electrical schematic"* and a layout example in *Figure 28: "HDMI2C1-6C1 layout example"*.

Either HSP053-4M5, HSP051-4M10 or ECMF04-4HSWM10 can be used to protect TMDS lanes against ESD.

Figure 27: HDMI2C1-6C1 electrical schematic

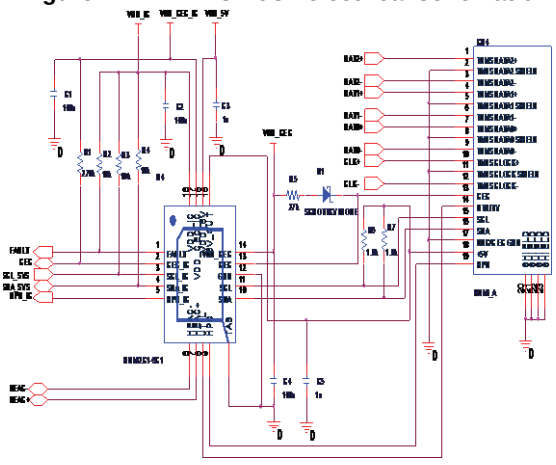
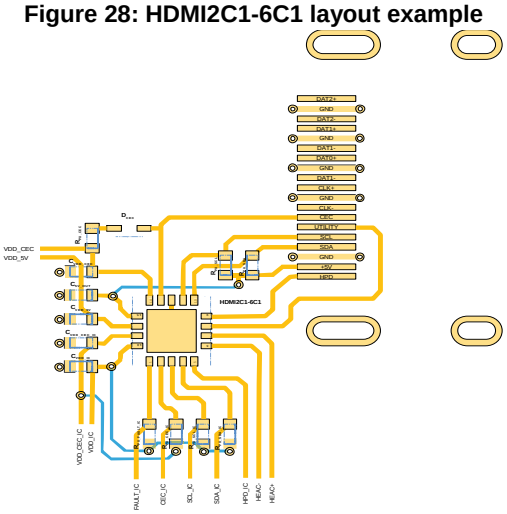


Figure 28: HDMI2C1-6C1 layout example



The HDMI2C1-6C1 is fully compliant with HDMI 1.4b standard requirements.

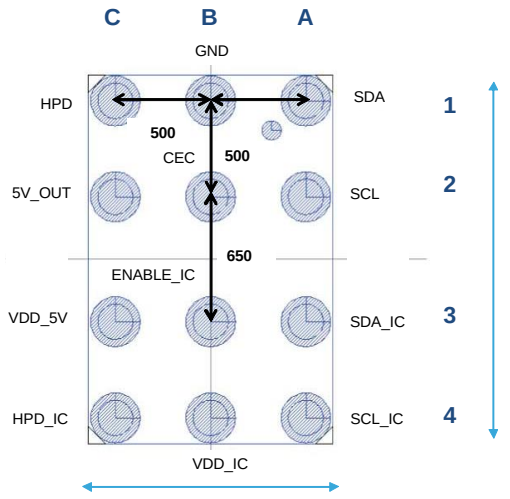
5.2.1.2 HDMI2C4-5F2

The HDMI2C4-5F2 provides ESD protection on all HDMI connector control pins, and integrates level shifter, signal conditioning and dynamic pull-up on DDC pin in Flip Chip package. It also integrates current limiter and short-circuit protection on + 5 V power pin.

The HDMI2C4-5F2 is dedicated to HDMI source device.

Figure 29: HDMI2C4-5F2 package

Figure 30: HDMI2C4-5F2 pin-out, bump side



The ENABLE_IC pin is used to enable or disable level shifters on DDC bus and on HPD line to reduce power consumption in standby mode. Setting the ENABLE_IC pin to low level disables all integrated level shifter and disconnects 5V_OUT pin from VDD_5V.

The HDMI2C4-5F2 provides ESD protection on CEC line without level shifting.

The typical electrical layout and an example of layout are shown in *Figure 31: "HDMI2C4-5F2 electrical schematic"* and *Figure 32: "HDMI2C4-5F2 layout example"*.

Either HSP053-4M5, HSP051-4M10 or ECMF04-4HSWM10 can be used to protect TMDS lanes against ESD.

Figure 31: HDMI2C4-5F2 electrical schematic

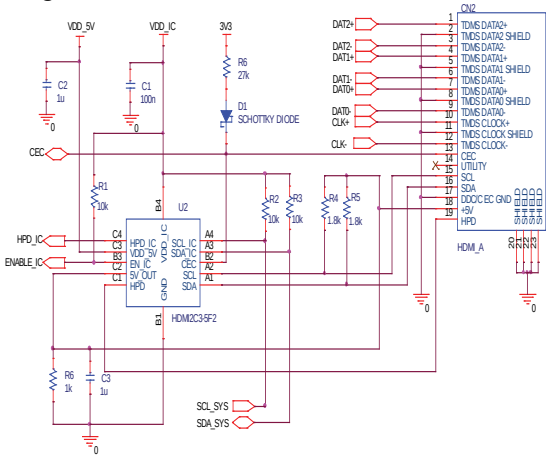
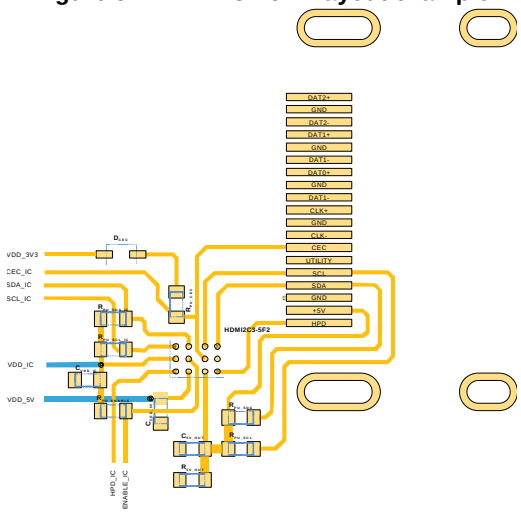


Figure 32: HDMI2C4-5F2 layout example



The HDMI2C4-5F2 is fully compliant with HDMI 2.0 standard requirements.

5.2.2 Full port protection

5.2.2.1 HDMI2C1-14HD

The HDMI2C1-14HD provides ESD protection for all HDMI connector pins and provides signal conditioning for control link of HDMI source in a single QFN36 lead package with 500 µm pitch. It integrates a current limiter and short-circuit protection on the + 5 V power pin.

Figure 33: HDMI2C1-14HD package

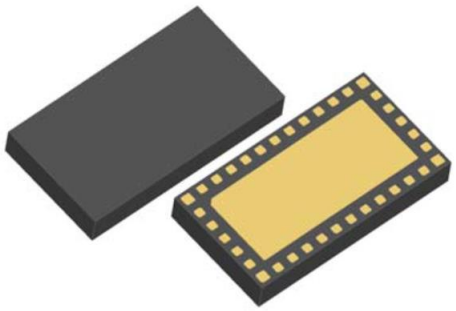
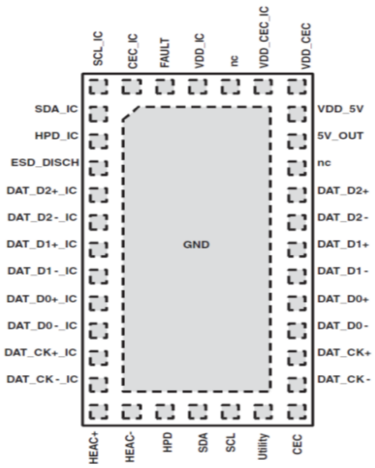


Figure 34: HDMI2C1-14HD pinout, top view



Its high frequency bandwidth and low clamping voltage on TMDS lines ensure the compatibility with the highest resolution of HDMI standard.

Figure 35: HDMI2C1-14HD, differential attenuation Sdd 21 typical value

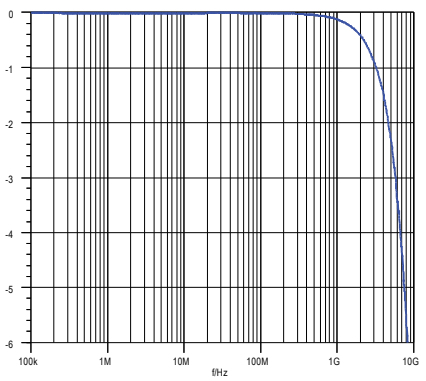
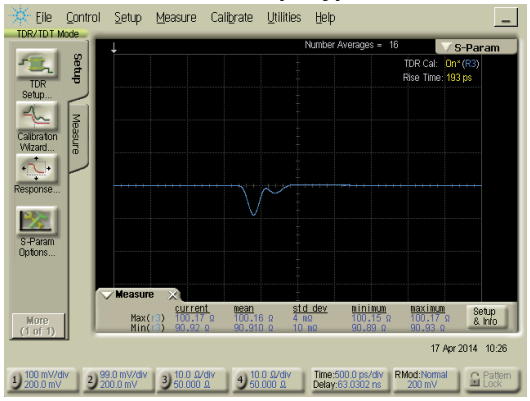


Figure 36: HDMI2C1-14HD, TDR on TDMS lane tr 10%-90% = 200 ps,typical value



The eye diagrams shown in *Figure 37: "Eye diagram at 3.4 Gbps, without HDMI2C1-14HD"* and *Figure 38: "Eye diagram at 3.4 Gbps, with HDMI2C1-14HD"* highlight a very low impact on signal transmission ensuring a good signal integrity.

Figure 37: Eye diagram at 3.4 Gbps, without HDMI2C1-14HD

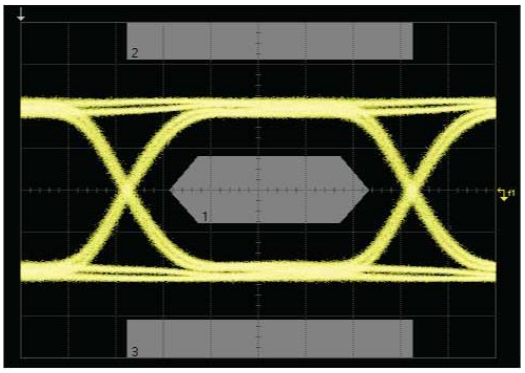


Figure 38: Eye diagram at 3.4 Gbps, with HDMI2C1-14HD

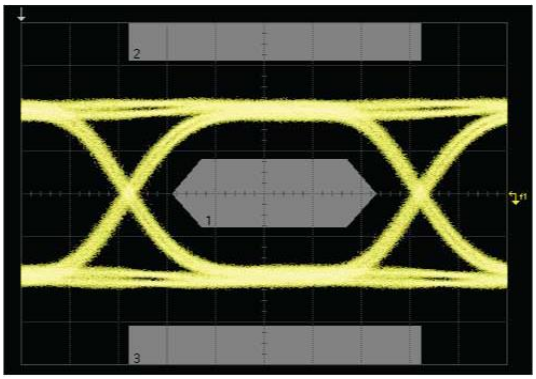


Figure 39: Eye diagram at 5.94 Gbps, without HDMI2C1-14HD

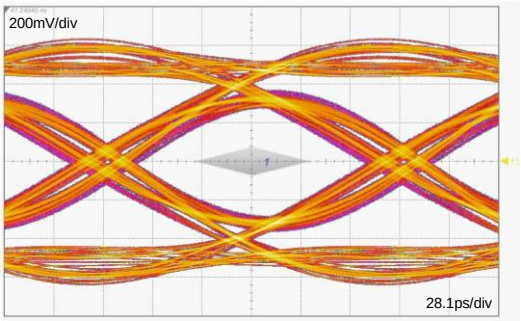
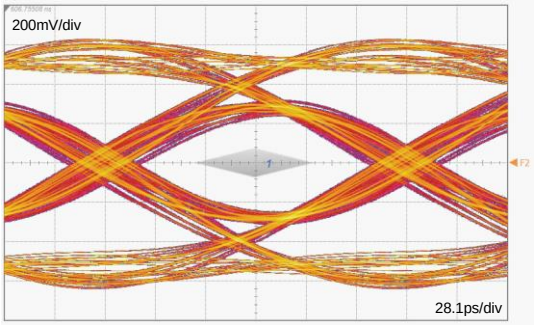


Figure 40: Eye diagram at 5.94 Gbps, with HDMI2C1-14HD



The active low fault pin is used to indicate a short-circuit or an overtemperature protection activation on 5V_OUT pin.

The typical electrical schematic is given in *Figure 41: "HDMI2C1-14HD electrical schematic"* and a layout example in *Figure 42: "HDMI2C1-14HD layout example"*.

Figure 41: HDMI2C1-14HD electrical schematic

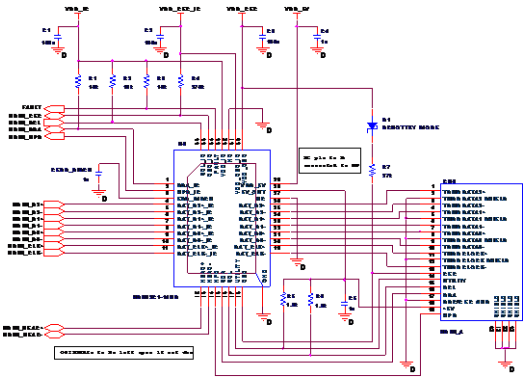
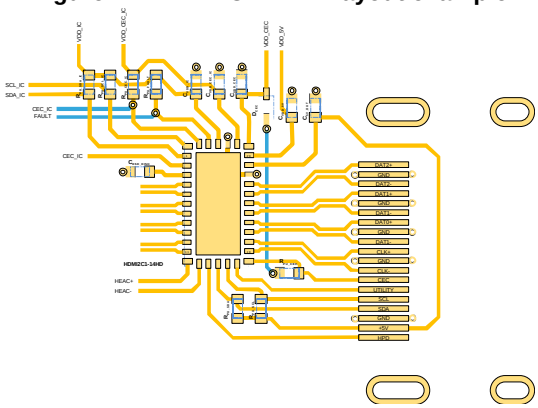


Figure 42: HDMI2C1-14HD layout example



The HDMI2C1-14HD is compliant with HDMI 2.0 standard requirements.

5.2.2.2 HDMI2C1-14HDS

The HDMI2C1-14HDS provides ESD protection for all HDMI connector pins and provides signal conditioning for control link of HDMI source in a single QFN24 lead package with 500 µm pitch. It integrates a current limiter and short-circuit protection on the +5 V power pin.

The HDMI2C1-14HDS is dedicated to HDMI source devices.

Figure 43: HDMI2C1-14HDS package

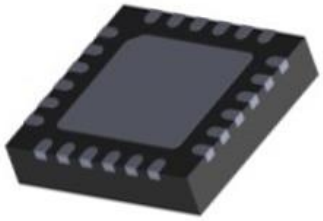
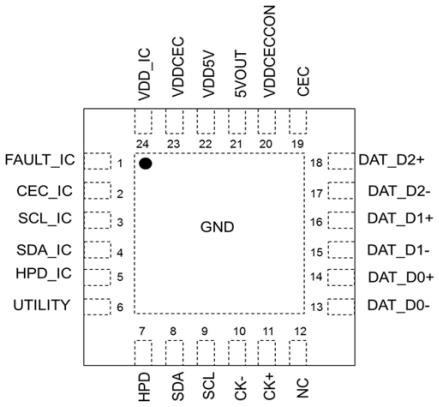


Figure 44: HDMI2C1-14HDS pinout, top view



Its high frequency bandwidth and low clamping voltage on TMDS lines ensure the compatibility with the highest resolution of HDMI standard.

Figure 45: HDMI2C1-14HDS differential attenuation Sdd21 typical value

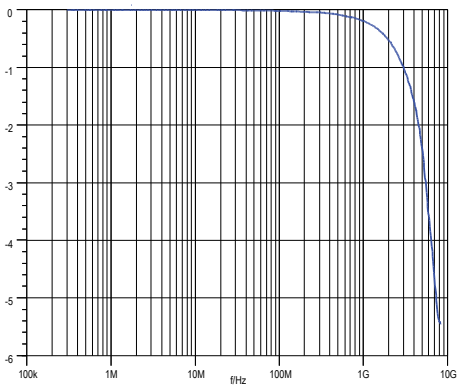
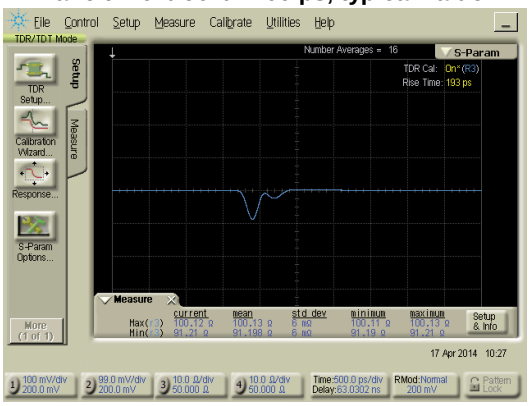


Figure 46: HDMI2C1-14HDS, TDR on TDMS lane tr 10%-90%= 200 ps, typical value



The eye diagrams shown from *Figure 47: "Eye diagram at 3.4 Gbps, without HDMI2C1-14HDS"* to *Figure 50: "Eye diagram at 5.94 Gbps, with HDMI2C1-14HDS"* highlight a very low impact on signal transmission ensuring a good signal integrity.

Figure 47: Eye diagram at 3.4 Gbps, without HDMI2C1-14HDS

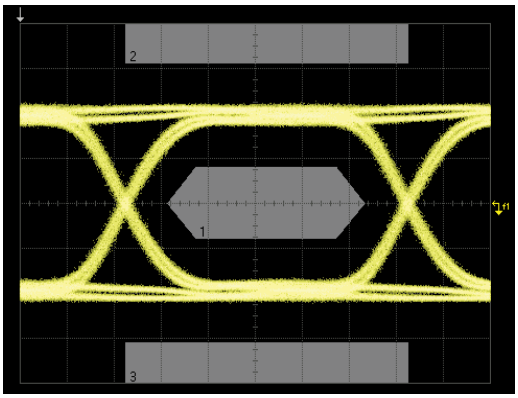


Figure 48: Eye diagram at 3.4 Gbps, with HDMI2C1-14HDS

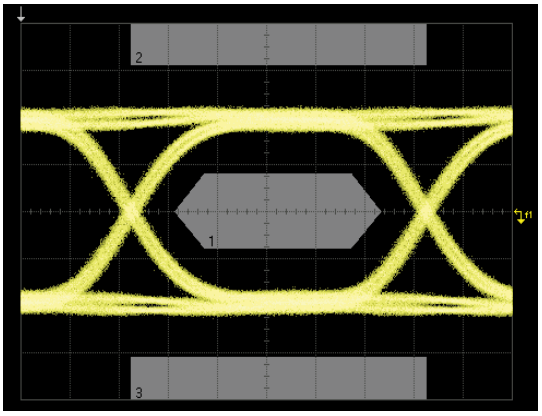


Figure 49: Eye diagram at 5.94 Gbps, without HDMI2C1-14HDS

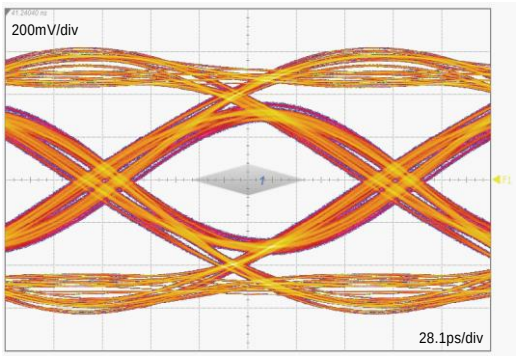
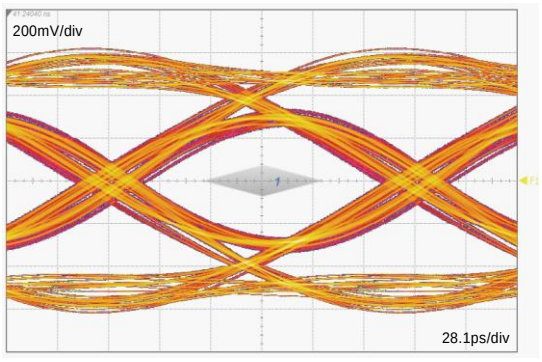


Figure 50: Eye diagram at 5.94 Gbps, with HDMI2C1-14HDS



The active low fault pin is used to indicate a short-circuit or an overtemperature protection activation on 5V_OUT pin.

The typical electrical schematic is given in *Figure 51: "HDMI2C1-14HDS electrical schematic"*.

Figure 51: HDMI2C1-14HDS electrical schematic

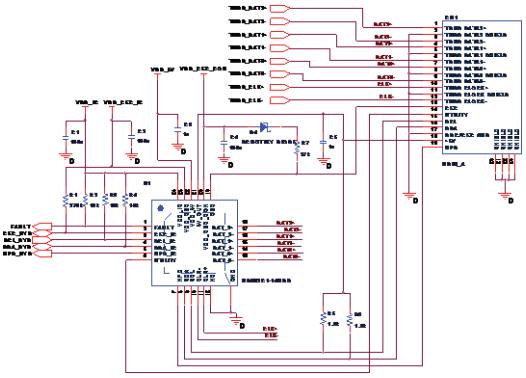
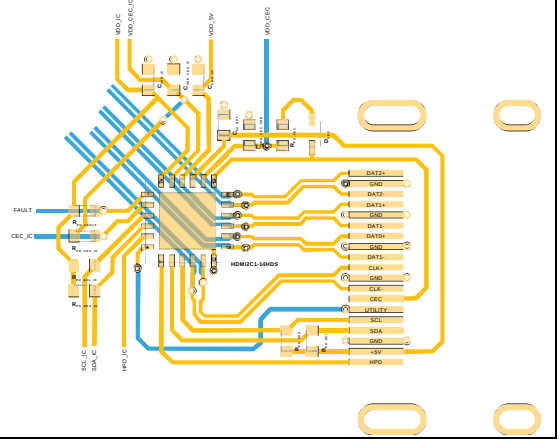


Figure 52: HDMI2C1-14HDS layout example



The HDMI2C1-14HDS is compliant with HDMI 2.0 standard requirements.

5.3 HDMI2Cx for HDMI™ sink device

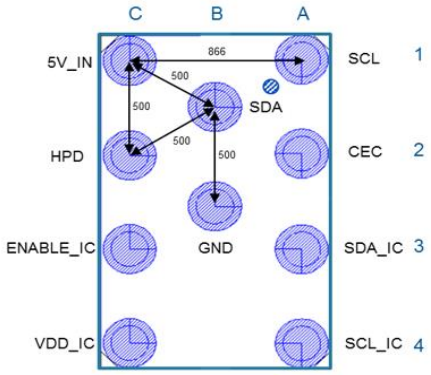
5.3.1 Control lines: HDMI2C2-5F2

The HDMI2C2-5F2 provides ESD protection on all HDMI connector control pins, and integrates level shifter, signal conditioning and dynamic pull-up on DDC pin in Flip Chip package.

The HDMI2C2-5F2 is dedicated to HDMI sink device.

Figure 53: HDMI2C2-5F2 package

Figure 54: HDMI2C2-5F2 pinout, bump side



The enable pin allows the + 5 V power pin to be sensed and/or the HDMI2C2-5F2 to be disabled so to reduce power consumption in standby mode. Setting the ENABLE_IC pin to low level disables all integrated level shifters and disconnects 5V_OUT pin from VDD_5V.

The typical electrical schematic is given in *Figure 55: "HDMI2C2-5F2 electrical schematic"* and a layout example in *Figure 56: "HDMI2C2-5F2 layout example"*

Either HSP053-4M5, HSP051-4M10 or ECMF04-4HSWM10 can be used to protect TMDS lanes against ESD.

Figure 55: HDMI2C2-5F2 electrical schematic

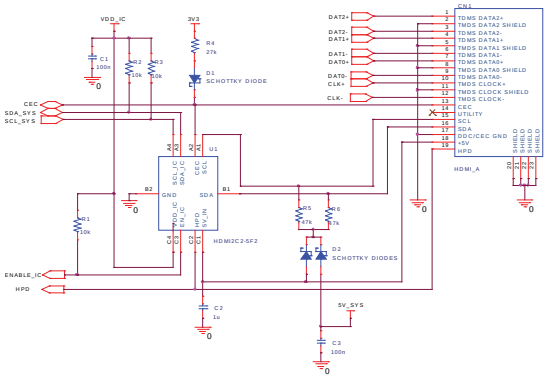
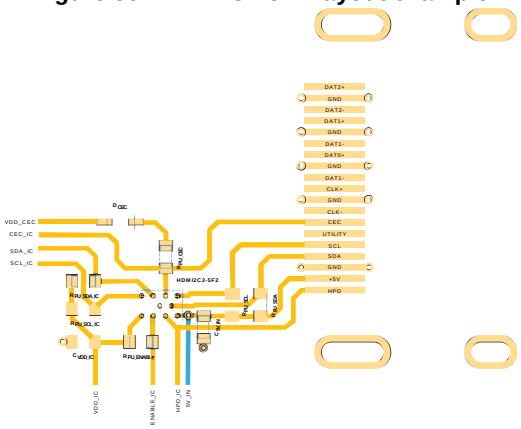


Figure 56: HDMI2C2-5F2 layout example



The HDMI2C2-5F2 is fully compliant with HDMI 2.0 standard requirements.

5.3.2 Full port protection: HDMI2C2-14HD

The HDMI2C1-14HD provides ESD protection for all HDMI connector pins and provides signal conditioning for control link of HDMI sink in a single QFN36 lead package with 500 µm pitch

Figure 57: HDMI2C2-14HD package

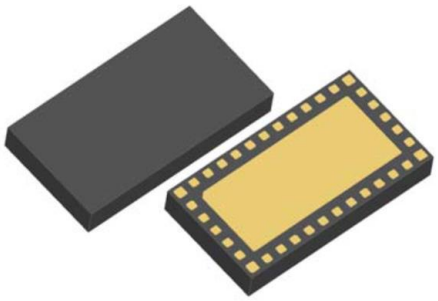
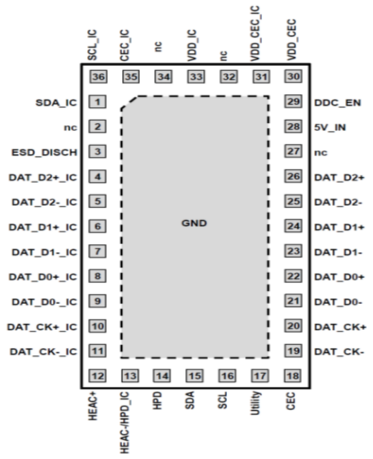


Figure 58: HDMI2C2-14HD pinout, top view



Its high frequency bandwidth and low clamping voltage on TMDS lines ensure the compatibility with the highest resolution of HDMI standard.

Figure 59: HDMI2C2-14HD, differential attenuation Sdd 21 typical value

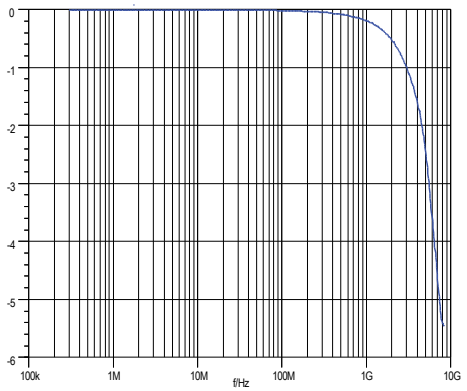
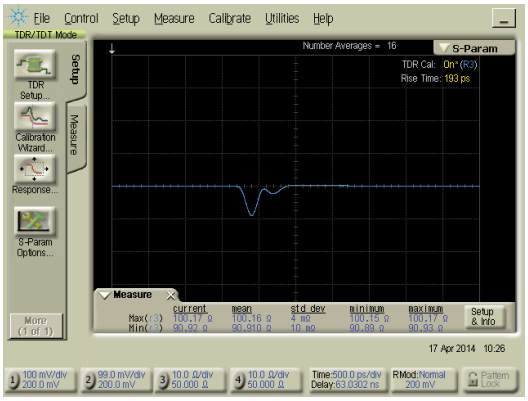


Figure 60: HDMI2C2-14HD, TDR on TDMS lane tr 10%-90% = 200 ps, typical value



The eye diagrams shown from *Figure 61: "Eye diagram at 3.4 Gbps, without HDMI2C2-14HD"* to *Figure 64: "Eye diagram at 5.94 Gbps, with HDMI2C2-14HD"* highlight a very low impact on signal transmission ensuring a good signal integrity.

Figure 61: Eye diagram at 3.4 Gbps, without HDMI2C2-14HD

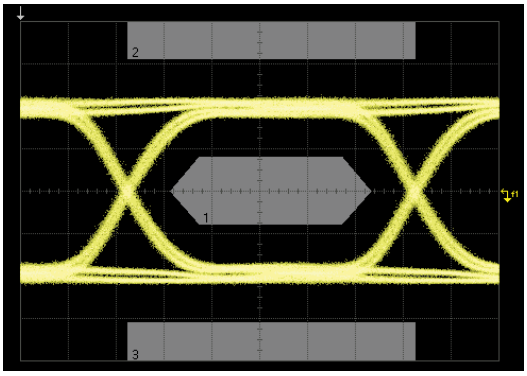


Figure 62: Eye diagram at 3.4 Gbps, with HDMI2C2-14HD

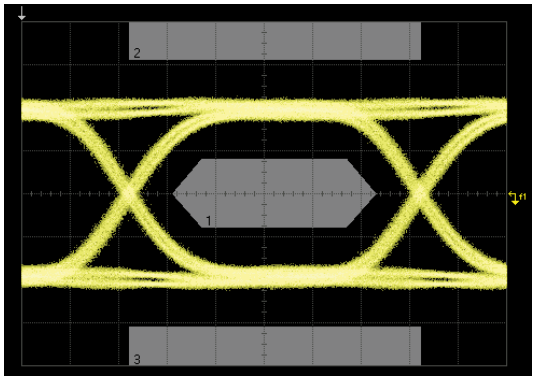


Figure 63: Eye diagram at 5.94 Gbps, without HDMI2C2-14HD

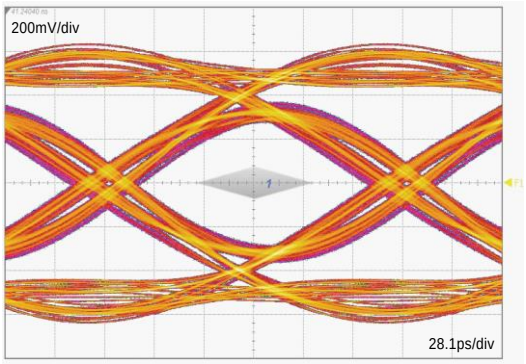
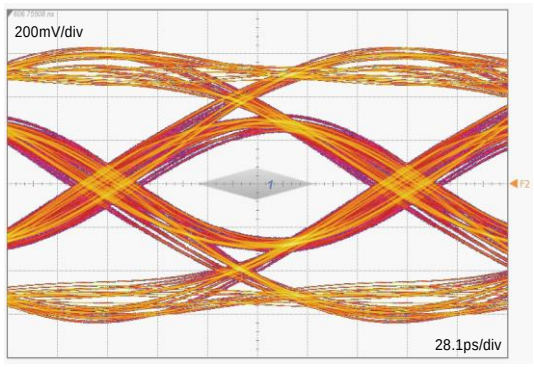


Figure 64: Eye diagram at 5.94 Gbps, with HDMI2C2-14HD



The active low fault pin is used to indicate a short-circuit or an overtemperature protection activation on 5V_OUT pin.

The typical electrical schematic and an example of layout are shown below, see *Figure 65: "HDMI2C2-14HD electrical schematic"* and *Figure 66: "HDMI2C2-14HD layout example"*.

Figure 65: HDMI2C2-14HD electrical schematic

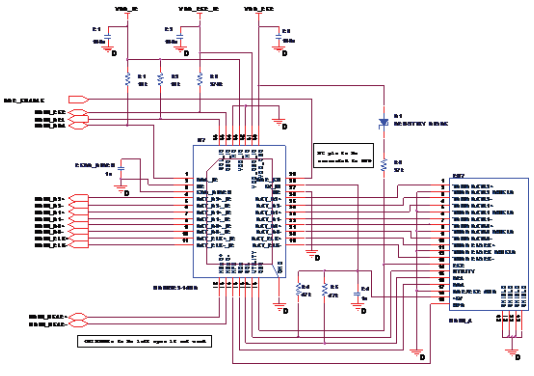
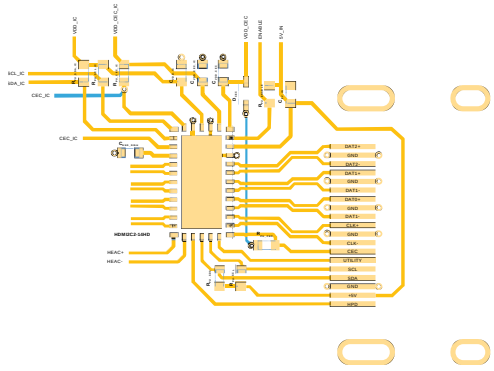


Figure 66: HDMI2C2-14HD layout example



The HDMI2C2-14HD is fully compliant with HDMI 2.0 standard requirements.

6 Conclusion

Consumer applications as set-top boxes fulfill EMC requirements as described in CISPR 20/EN 55020 or CISPR 24/EN 55024. In particular ESD robustness test has to be performed on HDMI port.

An HDMI port is composed of several links with different electrical characteristics introducing specific constraints on ESD protection devices.

This application note presents STMicroelectronics offering for HDMI port: standalone ESD protection for TMDS lines and ESD protection with signal conditioning for control lines or for the whole HDMI port. The high frequency bandwidth of ESD protection for TMDS line ensures a low impact of the protection device on signal integrity. The signal conditioning and the dynamic pull-up on the DDC bus help the system to drive high capacitive cables by respecting the standard requirements.

7 Revision history

Table 8: Document revision history

Date	Revision	Changes
04-Dec-2017	1	Initial release.

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